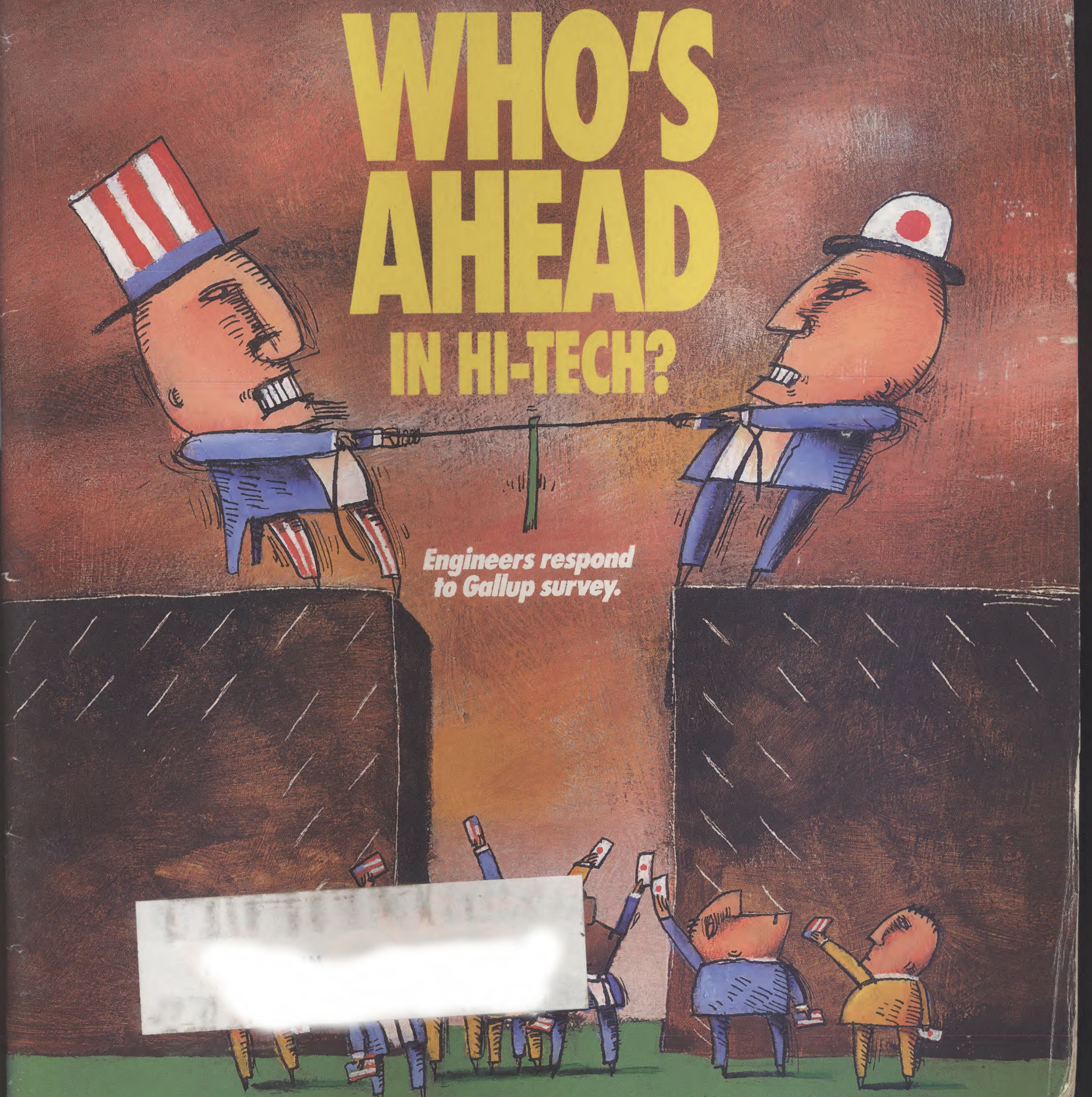
SPECIAL **WORKSTATIONS** GUIDE P.31

IEEE
SPECTRUM

WHO'S AHEAD IN HI-TECH?

Engineers respond to Gallup survey.



APRIL 1991 THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

Newslog

FEB 12. Finland's **Nokia Mobile Phones** said it would buy **Technophone**, based in Camberley, England. This merger will create a cellular phone manufacturer second in size only to Japan's **NEC Corp.**

FEB 13. The **Federal Communications Commission**, Washington, D.C., said it would allow a third mobile telephone service in six cities. The action enables **Fleet Call Inc.**, Bloomfield, N.J., a provider of private radio service for taxi fleets and delivery services, also to offer mobile phone services to individuals. Using advanced digital transmission techniques to increase the number of calls over its radio frequencies, Fleet Call plans to build systems in New York City, San Francisco, Los Angeles, Chicago, Dallas, and Houston, Texas.

FEB 14. The **United States** and **Japan** began negotiations to extend the five-year-old semiconductor accord that, following U.S. complaints in the 1980s that Japan was dumping memory chips, was set up to improve U.S. access to the Japanese market. The pact ends in July.

FEB 14. Delegates from more than 100 nations, including the United States, formally adopted a pact that sets a framework to curb the threat of **global warming**. The agreement, reached during a 10-day international conference in Chantilly, Va., also established guidelines for assistance to less developed nations that could be harmed by the pact.

FEB 15. **U S West Inc.**, Englewood, Colo., said it would pay the US $10 million fine levied by the **U.S. Justice Department**—the largest antitrust fine ever—for violating the 1982 Modified Final Judgment. U S West was charged with selling special computerized consoles made by a former subsidiary and selling computerized switching services to the General Services Administration at prices lower than those offered by **AT&T Co.**

FEB 15. The first product that lets personal computers read handwritten Chinese and Japanese characters was introduced by **Apple Computer Inc.**, Cupertino, Calif., and **Communication Intelligence Corp.**, Menlo Park, Calif., in an effort to expand their markets overseas. The Mac Handwriter works with Apple's Macintosh.

FEB 19. The **Japanese Government**, reacting to a nuclear plant mishap that occurred on Feb. 9, announced new guidelines for shutting down nuclear power plants. The **Ministry of International Trade and Industry** said operations must cease whenever radioactivity rises 20 percent or more.

FEB 21. **Sharp Corp.**, Japan's largest maker of flat-panel display screens, said it would begin producing them in a new plant being built in Camas, Wash. The announcement, which came a week after the **U.S. Commerce Department** accused Japanese screen manufacturers of selling their products below market value, made it the first Japanese maker to move screen production to the United States.

FEB 21. **Poland's Communications Ministry** said **AT&T Co.** will invest in the country's telephone network—up to US $800 million, according to the official P.A.P. news agency.

FEB 22. The **Federal Communications Commission**, Washington, D.C., approved applications by three cable companies to build experimental telephone networks allowing people to use wireless telephones small enough to be carried in shirt pockets. To pick up the signals, **Cox Enterprises**, Atlanta, Ga.; **Cablevision Systems Corp.**, Woodbury, Long Island, N.Y.; and **Continental Cablevision Inc.**, Boston, will tie together scores of low-powered radio towers scattered throughout a city.

FEB 25. **Zenith Electronics Corp.**, Glenview, Ill., said it had sold nearly a 5 percent stake in the company to **Goldstar Co.** of South Korea—one of the first big investments by a Korean firm in a publicly traded U.S. company.

FEB 25. **Sun Microsystems Inc.**, Mountain View, Calif., and **Hewlett-Packard Co.**, Palo Alto, Calif., announced a joint effort to develop advanced software that will allow their and other companies' computers to work together. Their goal: to create a standard that will be selected by the **Object Management Group**, an organization of over 100 high-technology concerns that is trying to develop standards for object-oriented software.

FEB 26. Researchers at **Bell Communications Research Inc.**, Livingston, N.J., said they were using a laser instead of a quartz crystal to boost the speed of a computer's clock.

FEB 28. **Ing C. Olivetti SpA**, Turin, Italy, launched the first portable computers made in Europe by a European manufacturer. The company said it hopes its three notebook and two laptop models—made by a German subsidiary—will enable it to capture 10 percent of the European portable computer market—put at US $3 billion this year.

MAR 1. A Federal District judge in San Francisco ruled that the **Intel Corp.**, Santa Clara, Calif., was not entitled to trademark protection on the name of its 386 microprocessor on the grounds that 386 is a generic term. The ruling absolves **Advanced Micro Devices Inc.**, Sunnyvale, Calif., of trademark infringement and makes it easier for it and others to market chips compatible with the 386.

MAR 5. **The National Aeronautics and Space Administration**, Washington, D.C., submitted a revised plan for its orbiting space station to the **National Space Council**. The agency plans to reduce the station's size and cost, cut its astronaut crew in half, and make construction and repair easier.

MAR 5. The **British Government** said it would open the UK telephone network to competitors, including mobile and cable operators. The most obvious beneficiaries are the **seven U.S. Bell operating companies,** which have been buying shares in British cable-TV companies in anticipation of such a move.

MAR 6. **The U.S. Commerce Department** announced that 11 companies had been awarded $9 million in matching grants that are designed to foster innovative civilian technologies and restore U.S. competitiveness. The technologies included inexpensive flat-panel display screens, advanced X-ray lithography research, and advanced superconductor research.

MAR 6. **President George Bush** in an address to a joint session of the **U.S. Congress** said the war in the Persian Gulf between the U.S.-led coalition forces and Iraq was over. A day earlier, the Bush administration had opened a special office to help U.S. companies bid for billions of dollars in reconstruction contracts to be awarded by war-devastated Kuwait. Priorities include power systems and repairing the environment.

Preview.

APR 12. Testing will begin by the Federal Communications Commission's **Advisory Committee on Advanced Television Service** in Alexandria, Va., to adopt a U.S. high-definition TV standard. The tests are to last about one year.

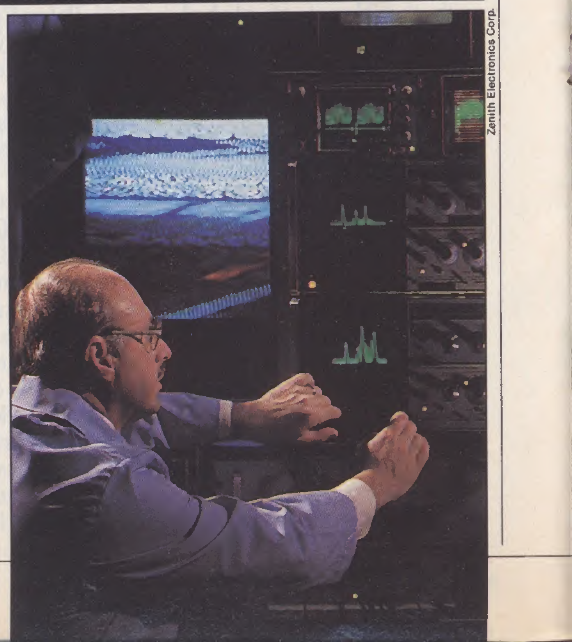
COORDINATOR: Sally Cahur

April 1991 Volume 28 Number 4

IEEE SPECTRUM

James Yang

CompuAdd Corp.



Zenith Electronics Corp.

CAREERS

PERSPECTIVE

Cover: Artist James Yang portrays the high-technology competition between Japan and the United States as a tug-of-war. The crowd symbolizes a sampling of IEEE members whom the Gallup Organization surveyed for opinions about which country leads. See p. 22.

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Forum

Whistle-blowing or hot air?

Some whistle-blowers have done quite well [''Whistle-blowing: not always a losing game,'' December, p. 49], but is that vindication? The three who quit General Electric Co.'s nuclear division in San Jose, Calif., got tremendous publicity through careful orchestration over the previous weeks, in order to capitalize on the news networks' eagerness to air their story.

At [Chicago-based] Commonwealth Edison Co., we were operating four 800-megawatt nuclear power reactors of the GE design that the three criticized. We took the media very seriously. We flew an engineer to Washington, D.C., to pick up the report. (With all their concerns about safety, the three did not see fit to tell the companies that were operating the plants about their concerns. If a utility knew of such safety concerns and did not report them promptly to the safety regulators, it would be subject to civil and criminal penalties.) As soon as a copy of the report reached Chicago, a team of 30 engineers worked through the night to see if any safety issue should dictate immediate shutdown of our plants. There was nothing.

We took the matter seriously because one of the GE engineers, Dale Bridenbaugh, had been on the start-up team for our Dresden 1 unit. Our people knew and respected Bridenbaugh. After the media splash, we learned that the three were members of a group called Creative Initiative that had taken a position on the nuclear shutdown initiative then on the ballot in California.

It became known that whatever his concerns with GE management over safety, Bridenbaugh had argued forcefully with Creative Initiative's leaders *against* taking a position in support of Proposition 15. (The proposition would have stopped nuclear power in California, and its backers were known to be organizing to use it as a springboard for similar initiatives in other states to stop completion of plants licensed for safety by the Nuclear Regulatory Commission.)

Perhaps the fact that whistle-blowers have made some money is the proper test. But I do not think so. (None of their ''safety concerns'' were new, and none resulted in any changes in designs or in any plants. Even Dresden 1, which went into operation a decade before most of the GE plants the three criticized, operated very safely for 25 years.) The income of MHB Technical Associates [the San Jose, Calif., consulting firm run by Bridenbaugh and his associates] has come from anti-nuclear groups, political state utility commissions, ombudsmen and opportunistic politicians, and the producers of *The China Syndrome*, not from anyone with actual responsibility for safety.

MHB's latest ''reactor safety study'' for the Union of Concerned Scientists was presented in Washington this past summer and sank like a stone. It contained no new or significant safety revelations. Its big claim, that the nuclear industry is promoting advanced reactors as ''inherently safe,'' is simply phony. As assistant secretary for nuclear energy at the U.S. Department of Energy in 1986, I stated my concerns about that meaningless term, and its use has been dropped by the Department of Energy, the nuclear industry, and the reactor designers.

Because these whistle-blowers have been able to make money, should they really be held up as role models for responsible, socially conscious engineers?

A. David Rossin
Los Altos Hills, Calif.

Education machinations

I read with interest the article ''Reversing sagging precollege skills in mathematics and science'' [December, pp. 44–47]. In ''Tying in the real world,'' many do not see the forest for the trees. Too much specialization and not enough generalization will not create enthusiasm for learning. Most of the good teachers and professors (as a Life Member I have had many) under whom I had the good fortune to study would try to link a problem to something in one's daily living. I think the education process today does not give children a good foundation.

In the example using potatoes, the baking-size potatoes should have been reduced to a much smaller size than shown, perhaps 80–100 cubic centimeters to be cooked to a done state if immersed in boiling water (wet heat) for half an hour.

Likewise, if these nice bakers were placed in a 250 °C oven (dry heat), they would all burst in about half an hour or less. Most cookbooks recommend a 163–177 °C oven. Perhaps the author meant a 150 °C oven in which the bakers, if not too large, might be done in an hour.

There are too many students going from grade school to high school who cannot add or multiply unless they use their calculator. Minds like these cannot be creative because they lack a good foundation.

Hobart B. Bunce
Hoffman Estates, Ill.

I am happy to see that the IEEE and other engineering societies are beginning to take an active part in precollege education. It is time that the users and practitioners take over control from the educational establishment.

There is one very simple reason why U.S. children do badly in math and why, in addition, an ever decreasing number of them go into math, science, and engineering: they get turned off by inept teaching, irrelevant course content, and ridiculous textbooks.

The fact is that the educators who set the syllabus, who write the textbooks, and who eventually teach math and science courses are mostly unfamiliar with their subject. All they know is what they read in other books, or hear from other educators. Instead of talking with scientists and engineers—people who use math all day and are most able to tell which math and science concepts are important and which are not—educators have become an isolated group that has gradually developed its own ideas of what and how it should teach.

Teachers' colleges deal mostly with how to teach, not what to teach. The medium is the message. If it's too hard to teach science, then let us teach the ''scientific method'' instead. If teaching physics or chemistry is too hard, let's make up something new to teach—perhaps ''earth science'' or ''environmental science'' will do as a good substitute. Any science can be used to teach the scientific method, right?

This is nothing but a cop-out. The result is that much of what children learn bears no relationship to the real world. Let me give some examples I have run across:

• Did you know that the dependent variable is the ''image,'' and the independent variable is the ''pre-image''? That is the terminology my son's high school math book uses.
• Did you know that a staircase is an excellent example of an inclined plane? That's what my daughter's physics book said.
• Did you know that the mechanical advantage of a single-speed bicycle is 11 or 12? If that physics workbook were right, all our tow trucks could be replaced by 10-speed bicycles.
• How about the high school computer teacher who cannot understand why an IBM PC cannot read an ASCII text file from an Apple II disk—after all, isn't ASCII supposed to be universal?
• I've run across college freshmen who thought 0.2 was a half, 0.3 was a third, and 0.4 was a quarter. Ask them to multiply 3 times 6, and they rush for their calculator. If they hit the wrong key and get 57, that

(Continued on p. 90)

Calendar

Meetings, Conferences and Conventions

APRIL

Rubber and Plastics Conference (IA); April 15–16; Quaker Square Hilton, Akron, Ohio; D. Babich, General Tire & Rubber Co., 1 General St., Akron, Ohio 44239; 216-798-2832.

Ninth Annual VLSI Test Symposium (COMP et al.); April 16–18; Bally's Park Place Casino Hotel, Atlantic City, N.J.; K. Chao, Johns Hopkins University, APL-Johns Hopkins Road, Laurel, Md. 20723; 301-953-6121; fax, 301-953-1093.

Electro/International (Region 1 et al.); April 16–18; Jacob K. Javits Convention Center, New York; Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, Calif. 90045; 213-772-2965; fax, 213-641-5117.

International Symposium on Power Semiconductor Devices (ED); April 22–24; Baltimore, Md.; M. Ayman Shibib, AT&T Bell Laboratories, 2525 N. 12th St., Reading, Pa. 19612; 215-939-6576.

10th International Symposium on Computer Hardware Description Languages and their Applications (IFIP et al.); April 22–24, Marseille, France; Ronald Waxman, Department of Electrical Engineering, Thornton Hall, University of Virginia, Charlottesville, Va. 22903-2442; 804-924-6086.

International Symposium on Subscriber Loops and Services–ISSLS '91 (COMM et al.); April 22–25; Raicongrescentrum Europapleien, Amsterdam, the Netherlands; Paul 't Hoen, PTT Netherlands, Box 39, 2260 AA Leidsehenam, the Netherlands; (31+70) 43 22 33; fax, (31+70) 43 21 40.

International Workshop: Quality of Telecommunications Services and Products (QAMC); April 23–25; Val David, Canada; V. Seshadri, Room 3J536, AT&T, Crawfords Corner Road, Holmdel, N.J. 07733.

Rural Electric Power Conference (IA); April 28–30; Hyatt Regency, Dearborn, Mich.; Alan Blackmon, Blue Ridge Co-op, Box 277, Pickens, S.C. 29671; 803-878-6326.

MAY

Industrial and Commercial Power Systems Conference–I&CPS '91 (IA); May 6–9; Airport Hilton, Memphis, Tenn.; Allan H. Long, Memphis Light, Gas, & Water Division, Box 430, Memphis, Tenn. 38101-0430; 901-528-4859.

Power Industry Computer Applications Conference–PICA '91 (PE); May 7–10; Hyatt Regency/Sheraton, Baltimore, Md.; William Keagle Jr., Baltimore Gas & Electric Co., Electric Test Facility–RBC, Box 1475, Baltimore, Md. 21203; 301-281-3788.

IEEE members attend more than 5000 IEEE professional meetings, conferences, and conventions held throughout the world each year. For more information on any meeting in this guide, write or call the listed meeting contact. Information is also available from: Conference Services Department, IEEE Service Center, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855; 908-562-3878; submit conferences for listing to: Rita Holland, *IEEE Spectrum*, 345 E. 47th St., New York, N.Y. 10017; 212-705-7569.

For additional information on hotels, conference centers, and travel services, see the Reader Service Card.

oks

rrison have gathered a ses illustrating "prob- ciety by computers." eter Neumann's contri- *Engineering Notes* and und newspaper reports, fter case of computer t, hacking, viruses, in- nputer malfunction, and ed problems. Descrip- the "gee-whiz" tone aper reports make the l easy to read, even for normally find such fare

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ts, however, lurk some For example, the pref- ace says the book was "designed with teaching purposes in mind in an effort to help rectify the shortage of texts" on computer ethics. This statement is surprising because the book contains few of the pedagogical aids usually found in a textbook. Though seven of the eight chapters do contain one scenario for the student to think about as homework, and one chapter suggests an in-class role-playing exercise, no other exercises or questions are presented at the end of each chapter.

Other areas where the book falls short include the scenario on software ownership, which is actually about logic bombs (pieces of code that initiate a destructive subroutine when certain conditions arise), and thus belongs in a different chapter. Also, the section on computers and elections is not about privacy, but rather about computer crime or malfunctions, and so belongs with these topics.

The book's most serious problem, however, is in the chapter on hacking. At the very least, a textbook should do no harm,

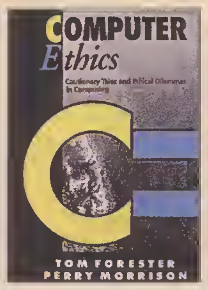
Books

Hackers or heroes?

Terrell Ward Bynum

This book has several virtues and a serious defect. The virtues would make it an attractive high school or college textbook. Indeed, the authors say their "simple aim" was "sensitizing undergraduate computer science students to ethical issues." With the aid of a competent teacher, *Computer Ethics* could no doubt achieve this modest goal. But the defect could make it a nuisance, even a danger, to student users, their schools, and possibly their communities.

Computer Ethics: Cautionary Tales and Ethical Dilemmas in Computing. *Tom Forrester and Perry Morrison, MIT Press, Cambridge, Mass., 1990, 193 pp., $19.95.*



Forrester and Morrison have gathered a treasure chest of cases illustrating "problems created for society by computers." Relying heavily on Peter Neumann's contributions to *Software Engineering Notes* and on various magazine and newspaper reports, they present case after case of computer crime, software theft, hacking, viruses, invasion of privacy, computer malfunction, and other computer-caused problems. Descriptions that often have the "gee-whiz" tone of sensational newspaper reports make the book entertaining and easy to read, even for students who might normally find such fare uninteresting.

Alongside these spicy accounts is the occasional helpful explanation or elaboration. For example, Chapter 2 on computer crime explains why reported crimes may be only "the tip of the iceberg," and Chapter 5 has one of the clearest explanations I have ever seen of why complex computer systems are often unreliable and plagued by bugs.

Among these merits, however, lurk some minor shortcomings. For example, the preface says the book was "designed with teaching purposes in mind in an effort to help rectify the shortage of texts" on computer ethics. This statement is surprising because the book contains few of the pedagogical aids usually found in a textbook. Though seven of the eight chapters do contain one scenario for the student to think about as homework, and one chapter suggests an in-class role-playing exercise, no other exercises or questions are presented at the end of each chapter.

Other areas where the book falls short include the scenario on software ownership, which is actually about logic bombs (pieces of code that initiate a destructive subroutine when certain conditions arise), and thus belongs in a different chapter. Also, the section on computers and elections is not about privacy, but rather about computer crime or malfunctions, and so belongs with these topics.

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Books

but I am frankly worried that *Computer Ethics* does not meet this basic requirement. Although it tries to give both sides of the argument about hacking, passages like this one on p. 60 stand out:

> "After all, when one 'breaks' into a system, nothing has been broken at all—hence there is no obvious intent to cause harm. When a file has been copied or selectively viewed, then what has been stolen? The information is, after all, still there. And if one happens to try out a few programs while browsing through a system, is this almost analogous to seeing someone's bicycle, riding it for a few meters and then putting it back? Again, what harm has been caused, what crime has been committed?"

The authors refer to those who engage in such "cracking" as "modern-day Robin Hoods":

> "Given that more and more information about individuals is now being stored on computers, often without our knowledge or consent, is it not reassuring that some citizens are able to penetrate these databases to find out what is going on? Thus it could be argued that hackers represent one way in which we can help avoid the creation of a more centralized, even totalitarian government."

They compare hackers with newspaper reporters defending freedom of the press or freedom of information, arguing that, "in a fair and open society," hacking that destroys nothing and steals nothing should be tolerated—indeed, that prevention of such hacking would be similar to racial, ethnic, or religious repression.

Chapter 4 also describes equipment needed for hacking, contains specific information on breaking into other people's computer systems, and lists detailed, "how-to" hackers' guidebooks for further reading.

For these reasons, I fear that this book may encourage some students to engage in illegal extracurricular activities—and do so self-righteously—under the mistaken impression that they are defending some noble cause.

A moment's reflection on so-called "harmless" hacking reveals the tremendous damage it can do. Is it okay, for example, to break into someone's computer and read unpublished manuscripts, a personal journal, or love letters? Should people have access to the computer systems of doctors, lawyers, banks, accountants, hospitals, psychiatrists? Is such behavior noble?

Is there any ethical difference between the burglar who, without breaking anything, enters a doctor's office, and reads confidential files, and the hacker who reads the same files by remotely "breaking into" the doctor's computer system? In both cases, an egregious violation of the right to privacy occurs. Was that right somehow repealed when computers were invented? Surely not.

Privacy is not some small thing to be sacrificed to a hacker's curiosity. It is a fundamental right, without which our quality of life would be seriously degraded. Yet some students who read this book may very well get the impression that intrusive forms of hacking are in some way noble activities.

For these reasons, I worry that *Computer Ethics*, if widely adopted as a textbook, could teach students more about hacking than about ethics. The first targets would be school computers, followed by other systems worldwide. And repercussions for the students, if caught, would be serious.

I hope it never comes to that.

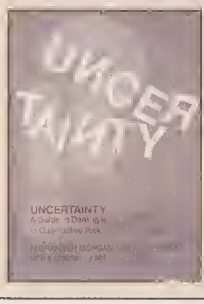
Terrell Ward Bynum is director of the Research Center on Computing and Society at Southern Connecticut State University in New Haven. He was editor of a special issue on computer ethics of the journal Metaphilosophy *(published in October 1985 by Basil Blackwell, Oxford, England), and will be co-chairman of a conference next August on "Computing and Values," funded by the National Science Foundation.*

Understanding uncertainty

Joseph Fragola

"The past decade has seen a growing recognition that policies that ignore uncertainties about technology, and about the physical world, often lead in the long run to unsatisfactory technical, social, and political outcomes," the authors note at the outset of this new contribution to the study of uncertainty and risk. They rightly attribute this change in perspective to the rising interest in the quantitative analysis and assessment of risk.

Uncertainty: A Guide to Dealing With Uncertainty in Quantitative Risk and Policy Analysis. *M. Granger Morgan and Max Henrion, Cambridge University Press, Cambridge, England, and New York, 1990, 250 pp., $44.50.*



The authors describe the general approaches and specific methodologies that deal with scientific and technical uncertainty in the areas of risk analysis, quantitative policy analysis, and policy-focused research. Their book covers the entire analysis process, whose basic steps are summarized in their conclusion: "identifying the sources of uncertainty, expressing them in the form of probability distributions, choosing appropriate computational methods for propagating uncertainty through the model to analyze its effects, and devising clear ways to communicate the results."

This undertaking is formidable not only because the subject is so current and the areas of application so broad, but also because of the diversity of the relevant audience—in both type and level of technical expertise. The book's potential audience runs the gamut from the risk or policy analyst to the administrative or policy decision-maker who is more interested in the strategic issue of when uncertainty is of interest in decision making.

The issues are introduced through three well-chosen case studies of recent major policy problems whose analysis involved techniques for explicitly treating uncertainty—a safety study by the U.S. Nuclear Regulatory Commission, an ambient-air-quality standards study by the Environmental Protection Agency, and an analysis of the depletion of stratospheric ozone by chlorofluorocarbons led by the National Academy of Sciences. Since these cover a variety of scientific fields, involve key policy issues, and are all publicly available, the reader has a ready reference if more details are desired.

The authors encapsulate each study nicely, highlighting the uncertainty-related issues of interest. All are short enough to merit a reading as a memory refresher, by even the seasoned risk analyst.

Chapter 3 is an overview of quantitative policy analysis. Again, for the experienced reader, it is a useful checklist for undertaking analysis and a reminder of the iterative nature of analysis. The newcomer will glean a good understanding of the framework of analysis, although the material is directed too much, perhaps, at policy-related studies and gives risk analysis and assessment too little attention.

The authors' attack on the problem of uncertainty begins in earnest in Chapter 4 when they introduce the nature of probability. They avoid wasting time on the arguments between the frequentists and Bayesians. They concisely note that the frequentists view probability from an "objective" perspective, and then unashamedly adopt the Bayesian view, which emphasizes the alternative "subjective" viewpoint.

Then they make the extremely important observation that in probabilistic analysis only *empirical* or *chance* quantities can properly be represented by subjective probability distributions, and it is generally inappropriate to represent uncertainty about decision variables and value parameters by probability distributions. This is a keen insight often missed by even veteran analysts.

Chapter 5 offers a short course in probability distributions and statistical estimation. While it is unlikely to serve as a solid foundation for those unfamiliar with these con-

Books

cepts, its many references will aid newcomers, and practitioners will find it a convenient reference. The next two chapters deal with the problem of using human judgment and assessing the uncertainty associated with these judgments.

Described in Chapter 8 are the various analytic and computational techniques available for examining certain inputs as they are propagated throughout a model. The treatment of the classic analytic methods is necessarily mathematical and essential even though it may lose nontechnical readers—decision-makers, for example. Though, as the authors point out, these methods are rarely useful beyond first-order assessments, they are wisely included for the sake of completeness.

The authors emphasize that while the discrete probability approach is now more popular, it becomes intractable with more than a dozen or so inputs. Thus, for complex analysis, use of the Monte Carlo method is on the rise, a practice that will continue as flexible Monte Carlo software becomes more available. This chapter also discusses the importance of software and refers to available packages.

Chapter 9 emphasizes the need to display results of analysis in such a way as to put them in the proper perspective. It should be of interest to any decision-maker who has ever had to decipher analysis data and communicate their essence to other policymakers or to the public.

Chapter 10, which explains a detailed application of a particular tool the authors use, comes across as a bit self-serving. It probably would have served readers better in an appendix.

However, the reader is not long disappointed because the next chapter reveals a keen insight into the actual uses of models. The authors point out that good analysts use models as tools in a sensitivity-driven iterative fashion and that for this reason, good analysts are hard to find, especially in regulatory bodies. Since such bodies are often the sponsors of the model, this often results in the development of large and complex models that include many superfluous features while excluding other features that are critical. The best way to use large, complex models in policy analysis, the authors say, is to abstract those portions that can provide the relevant empirically validated insights.

The final chapter addresses the limitations of analysis in light of uncertainties and the conditions under which ignoring these uncertainties can degrade the analytical and ethical correctness of the results.

This book is a significant contribution to the exploration of the basic issues and constitutes an important addition to the technical literature addressing uncertainty.

Joseph R. Fragola (SM), a 20-year veteran in the fields of reliability and risk analysis, is vice president and manager of the safety, reliability, and risk-assessment operation at Science Applications International Corp. (SAIC) in New York City. He is co-author of Human Reliability Analysis: A Systems Engineering Approach With Nuclear Power Plant Applications *(John Wiley & Sons, 1989). He coordinated the development of IEEE Standard 500, the Reliability Data Manual.*

COORDINATOR: Glenn Zorpette

Recent books

CLIST Programming. *Bosler, Kurt,* McGraw-Hill, New York, 1990, 303 pp., US $47.95.

Nonlinear Systems. Vol. II: Applications to Bilinear Control. *Mohler, Ronald R.*, Prentice-Hall, Englewood Cliffs, N.J., 1991, 213 pp., $48.

Calendar

(Continued from p. 8)

Textile, Fiber, and Film Conference (IA); May 8–9; Hyatt Regency, Greenville, S.C.; Phil Kemp, Electrical Systems Inc., Box 22548, Chattanooga, TN 37422; 800-366-6277.

Pacific Rim Conference on Communications Computers and Signal Processing (Victoria Section); May 9–10; Pan Agathoklis, Department of Electrical and Computer Engineering, University of Victoria, Box 3055, Victoria, B.C., Canada V8W 3P6; 604-721-8618.

Fourth IEEE Symposium on Computer-Based Medical Systems (COMP et al.); May 12–14; Stouffer Harborplace Hotel, Baltimore, Md.; Jeffrey Lesho, Johns Hopkins University, Johns Hopkins Road 13-5112, Laurel, Md. 20723-6099; 301-792-5000, ext. 8057.

41st Electronic Components and Technology Conference (CHMT); May 13–15; Westin Peachtree Plaza, Atlanta, Ga.; Jim Bruorton, c/o KEMET Electronics Corp., Box 5928, Greenville, S.C. 29606; 803-963-6621.

Custom Integrated Circuits Conference–CICC '91 (ED); May 13–16; Town & Country Hotel, San Diego, Calif.; Laura Morihara, Convention Coordinating, 47-344 Waihee Rd., Kaneohe, Oahu, Hawaii 96744; 808-239-4790.

Fifth International Conference on Advanced Computer Technology–Compeuro '91 Reliable Systems and Applications (ED); May 13–16; Palazzo della Cultura e dei Congressi, Bologna, Italy; Sercoop Congressi, Via Crociali 2,40100, Bologna, Italy; (39+51) 300811.

Ideas in Science and Electronics Symposium and Exposition (IEEE Albuquerque et al.); May 14–16; Albuquerque Convention Center, New Mexico; Dave Smoker Communications, 218 Manzano, N.E., Albuquerque, N.M. 87108; 505-266-7292; or Charles E. Christmann, c/o ISE Inc., 8100 Mountain Rd. N.E., Suite 109, Albuquerque, N.M. 87110; 505-262-1023.

Instrumentation and Measurement Technology Conference (IMTC); May 14–16; Omni Hotel at CNN Center, Atlanta, Ga.; Robert Myers, 3685 Motor Ave., Suite 240, Los Angeles, Calif. 90034; 213-287-1463; fax, 213-287-1851.

International Conference on Acoustics, Speech and Signal Processing (SP); May 14–17; Sheraton Centre, Toronto, Ont., Canada; ICASSP '91, c/o Southex Exhibitions, 1450 Don Mills Rd., Don Mills, Ont., Canada, M3B 2X7; 416-445-6641; fax, 416-442-2207.

Vehicular Technology Conference (VT et al.); May 19–22; Sheridan West Port Inns, Maryland Heights, Mo.; Jay Underdown, 58 Judy Dr., St. Charles, Mo. 63301; 314-946-9980 (O); 314-723-4200 (H).

International Semiconductor Manufacturing Science Symposium (ED); May 20–22; San Francisco Airport Hilton Hotel, San Francisco; Corinne Cargnoni, SEMI, 805 E. Middlefield Rd., Mountain View, Calif. 94043; 415-940-6950.

National Aerospace and Electronics Conference–NAECON '91 (AES et al.); May 20–24; Dayton Convention Center, Ohio; Sue Brown, ASD/ENES, Wright-Patterson AFB, Ohio 45433-6503; 513-255-6281.

Appliance Industry Conference (IA); May 21–22; University of Wisconsin, Madi-

(Continued on p. 14D)

Calendar

(Continued from p. 14B)

son; Otto Ehrsam, Bethlehem Steel Co., 701 E. Third St., Bethlehem, Pa. 18016; 215-694-6585.

Annual IEEE/ASME Joint Railroad Conference (IEEE et al.); May 21–23; Sheraton Westport Inn, St. Louis, Mo.; Robert B. Fisher, Land Transportation Division, Southeastern Pennsylvania Transportation Authority, 5800 Bustleton Ave., Philadelphia, Pa. 19149; 215-580-4888.

International Symposium on VLSI Technology, Systems, and Applications (ED); May 22–24; Lai Lai Sheraton Hotel, Taipei, Taiwan; Alice Chiang, Lincoln Laboratory, MIT, 244 Wood St., Lexington, Mass. 02173-0073; 617-981-0711.

Mediterranean Electrotechnical Conference (Region 8); May 22–24; Ljubljana; Baldomir Zajc, Fakuteta za Elektrotehniko, Trzaska 25, 61000 Ljubljana, Yugoslavia.

International Workshop on VLSI Process and Device Modeling (ED); May 26–27; Oiso Prince Hotel, Kanagawa, Japan; Hiroshi Iwai, Toshiba Corp., 1 Komukai, Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan; (81+44) 549 2266.

VLSI Technology Symposium (ED); May 28–30; Oiso Prince Hotel, Kanagawa, Japan; Dirk Bartelink, Hewlett-Packard Co., 3500 Deer Creek Rd., Palo Alto, Calif. 94304; 415-857-5364.

35th International Symposium on Electron, Ion and Photon Beams (ED); May 28–31; Seattle Sheraton Hotel and Towers, Wash.; J. Shaw, IBM Corp., T.J. Watson Research Center, Room 17-259, Yorktown Heights, N.Y. 10598; 914-945-2528.

Conference on Computers, Power and Communications in a Rural Environment–Wescanex '91 (Region 7 et al.); May 29–30; Delta Regina Hotel, Regina, Sask., Canada; Bill Kennedy, Saskatchewan Power Corp., 2025 Victoria Ave., Regina, Sask., Canada S4P 0S1; 306-566-2106.

45th Annual Symposium on Frequency Control (UFFC); May 29–31; Marriott Los Angeles Airport, California; Raymond L. Filler, U.S. Army Electronics and Technical Devices Laboratory, SLCET-EQ, Fort Monmouth, N.J. 07703; 908-544-2467.

JUNE

Fourth International Conference on Industrial and Engineering Applications of Artificial Intelligence and Expert Systems (COMP et al.); June 2–5; Waiohai Hotel, Kauai, Hawaii; Moonis Ali, University of Tennessee Space Institute, MS15, B.H. Goethert Parkway, Tullahoma, Tenn. 37388; 615-455-0631, ext. 236; fax, 615-454-2354.

Intensive Course on Electrical Contacts (IEEE/CHMT); June 3–7; Radisson Plaza Raleigh, Raleigh, N.C.; IEEE Holm Conference Registrar, 445 Hoes Lane, Box 1331, Piscataway, N.J. 08855-1331; 908-562-3863; fax, 908-562-1571.

Pulp and Paper Industry Conference (IA); June 3–7; Hotel des Gouverneurs Le Grand, Montreal; Michel Riverin, Relcon Inc., 0403 Clement St., Montreal, Que., Canada H8R 4B4; 514-595-5999; fax, 514-595-5680.

International Conference on Consumer Electronics (IEEE et al.); June 5–7 (Educational Session, June 4); Westin Hotel O'Hare, Rosemont, Ill.; Diane D. Williams, 67 Raspberry Patch Dr., Rochester, N.Y. 14612; 776-865-2938.

Microwave and Millimeter-Wave Monolithic Circuits Symposium (ED); June 9–10; Hynes Convention Center, Boston; Charles Huang, Anadigics Inc., 35 Technology Dr., Warren, N.J. 07060; 201-668-5000.

VLSI Multilevel Interconnection Conference (VMIC) (ED); June 10–13; Santa Clara Marriott Hotel, California; Thomas Wade, Engineering Dean's Office, University of South Florida, 4202 Fowler Ave., Tampa, Fla. 33620; 813-974-3786.

International Microwave Symposium–MTT '91 (MTT); June 11–13; Hynes Convention Center, Boston; Peter Staecker, MA-COM, M/S 704, 52 South Ave., Burlington, Mass. 01803; 617-272-3000, ext. 1602.

Ninth Biennial University/Government/Industry Microelectronics Symposium (ED); June 12–14; Florida Institute of Technology, Melbourne; Darlene Kirschner, Florida Institute of Technology, 150 W. University Blvd., Melbourne, Fla. 32901; 407-768-8000, ext. 8763.

Second International Conference on Magnetic Recording Systems (MAG et al.); June 12–15; Hidden Valley Retreat, Pittsburgh; Gordon Hughes, Seagate Technology, 900 Disc Dr., Scotts Valley, Calif. 95066; 408-439-2626; fax, 408-438-4190.

Device Research Conference (ED); June 16–19; University of Colorado, Boulder;

(Continued on p. 86B)

Speakout

The politics of science

There is general agreement among economists that research and development are key to economic growth. Japan's economic success, for example, is attributable to its better exploitation of technology (much of which originated in the United States). In the past decade, the Reagan and Bush administrations have provided increasing levels of support for U.S. R&D. But the U.S. economy has stagnated. Why?

First, President Reagan expanded defense R&D while leaving civilian R&D virtually flat. Second, driven by a "free-enterprise" ideology, the Republican administrations have refused to adopt any form of industrial R&D policy. Rather, they have accepted the premise that the Government should support fundamental research and so-called "generic" technology, leaving commercial applications to the private sector, which has failed to respond.

This second policy has led to massive Government investment in some large R&D projects associated with negligible economic benefits. Witness the Superconducting Super Collider. Its projected cost has tripled to some US $12 billion.

Consider, too, the National Aeronautics and Space Administration's space station Freedom. Until its recent downsizing, its cost of $30 billion was more than triple its original $8 billion estimate. The only projected economic benefit would be that associated with crystal growth in zero gravity. Such programs will not reestablish the United States' economic preeminence.

The Republican administrations' more traditional support of "little science" has not been much more productive economically. But here the scientific community itself bears at least partial responsibility. Scientists, as distinct from engineers, have forcefully advocated Government support of basic, as distinct from applied, research.

Although basic research almost always eventually results in some economic benefit, the time lag between the research and the ultimate benefit is often an appreciable part of a century. In today's economic climate we literally cannot afford to wait that long. The Government must alter its R&D funding policy to emphasize applied rather than fundamental research.

Before the United States became a debtor nation, in what were then science's "golden days," there was little need to prioritize R&D proposals; there was enough money for all. Today our budget deficit forces the United States to choose between alternative projects.

NO PRIORITIES. Yet both the Government and the scientists have failed to assess priorities. The National Academy of Sciences was once invited to prioritize the nation's R&D programs. The result was a limp categorization, carefully designed not to antagonize any sector of the scientific community. The simple fact is that the scientists have such vested interest in the Government's R&D programs that they cannot objectively discriminate among competing alternatives.

R&D priority decisions ultimately must be left to Congress. Prioritization implies policy, and policy is the responsibility of Congress. But, with few exceptions, members of Congress and their staffs are not technically trained; a way is needed to facilitate Congressional R&D prioritization.

Although the concept of a "science court" has never been popular, something like it might benefit Congress. Prioritization is necessarily an adversarial process. Congressmen, as lawyers, are familiar with such proceedings. A Congressional hearing resembling a science court may offer the needed prioritization mechanism.

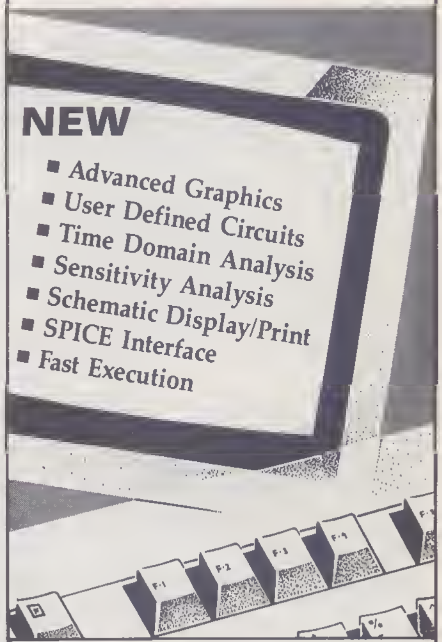
For two years the Carnegie Commission on Science, Technology, and Government has been studying the organization of science and technology in government. Its conclusions are due in another year or so. But the experience of the Commission's eminent members renders its recommendations almost a foregone conclusion; the nation should return to the glory days of the President's Science Advisory Council (PSAC) and an influential President's Science Advisor.

CLASSIC PATTERN. But though that golden age is past, the Bush administration has in effect organized R&D in the classic pattern. An eminent academician was named science advisor and promoted in rank to assistant to the President for science and technology, and the PSAC has become the PCAST (President's Council of Advisors on Science and Technology).

Just as centralized industrial planning is anathema to this Administration, so, too, is centralized technical organization to the academicians. There are four reasons for their aversion.

First, the scientists prefer multiple funding agencies because of the many opportunities they offer for proposal support.

Second, the scientists are accustomed to



Speakout

independence and resent centralized authority. A Federal department of science and technology is seen as a threat to academic freedom.

Third, the scientists are justly suspicious of the influence of a single scientist upon a technically untrained politician, be he President, Senator, or Congressman.

Fourth, it is argued that science and technology are concerns of almost all Government departments. Consequently, central R&D direction would infringe upon each department's jurisdiction and operation. But the Office of the Attorney General proves the fallacy of that argument; all Government agencies are concerned with the law, but the office provides support to all while also administering its own legal program.

It would be both easy and efficient to combine into one Department of Science and Technology: NASA, the National Science Foundation, the National Institutes of Health, the National Institute of Standards and Technology (the former Bureau of Standards), and the National Oceanic and Atmospheric Administration, together with the Department of Energy's Office of Energy Research and national laboratories (such as Argonne, Brookhaven, Fermi, and Oak Ridge). The resulting department would have a budget on the order of $25 billion and commensurate political clout.

Effective allocation of the nation's vast R&D resources demands centralized authority. If the United States is to exploit its R&D potential to the fullest, and if science and technology are ever to attain the political influence commensurate with their economic importance, organization of such a department is a *sine qua non.*

NEW ROLES. The time is also ripe for more U.S. engineers and scientists to present themselves for possible election to public office. The late Lord Snow achieved a certain celebrity with his identification of two often uncommunicating cultures: those of the humanities-trained lawyer and the technically trained engineer or scientist. The gulf between these two cultures has continued from Snow's day to the present; it is an obstacle to economic growth. If policy is to exploit technology, that gulf must be bridged.

What is needed are true political-scientists: engineers and scientists who are also politicians. John F. Kennedy once described his science advisor, Jerome Wiesner, as the only real political scientist in the White House. There have been others, notably James H. Killian and Vannevar Bush, who was the archetype. The United States needs more such scientists and engineers.

George C. Sponsler

George C. Sponsler is chairman of the IEEE-USA Aerospace R&D Policy Committee.

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Innovations

Building a better incandescent light bulb

A lamp that recycles its own previously wasted infrared energy has realized the old dream of a highly efficient incandescent bulb. Chemist John Ackerman and chemical engineer Himanshu Vakil developed it at the General Electric Research and Development Center in Schenectady, N.Y.

Incandescent bulbs, while popular for their pleasant light, are grossly inefficient: they radiate 75–80 percent of their electric energy input as heat. While heating a tungsten filament to a temperature higher than the average 2700 °C standard in current bulbs would cause it to radiate more of its energy at shorter, visible wavelengths, that also significantly shortens the lamp's life.

In theory, the filament could be kept at its operating temperature by being encased in a "thermal blanket" that reflected its own infrared radiation, thus reducing the amount of line current required to keep it hot. Indeed, people have known for decades how to devise coatings that can reflect infrared wavelengths while transmitting visible wavelengths. These coatings, called dielectric interference filters, are made by depositing alternating layers of materials with a high and a low index of refraction.

But no manufacturable version of the process has existed to date, said Vakil. Each layer some 100 nanometers thick must be uniform to an accuracy of 0.2 nm over the light bulb's curved surface. Moreover, the technique has to be repeatable so the bulbs' color, brightness, and efficiency are constant.

To meet those challenges, the GE scientists devised a variation of standard chemical vapor deposition techniques. The coating consists of alternating layers of metal oxides of high and low refractive indices, which Vakil would not identify since they are proprietary.

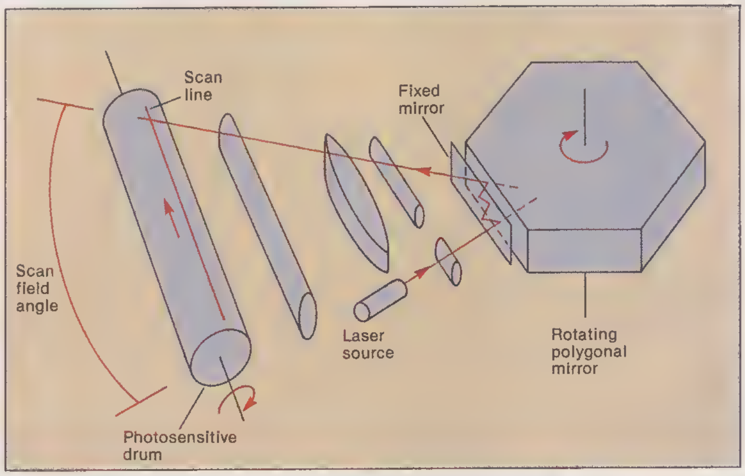
In addition, Ackerman and Vakil reshaped the bulb to focus the infrared radiation back onto the filament. And the filament itself had to be redesigned to draw lower line current.

The first commercial lamp came on the market last year: a new family of incandescent lamps known as Halogen IR PAR 38 (parabolic aluminum reflector) lamps, available in spot and flood versions for industrial and office use. The new 60-watt Halogen IR lamp can provide the same amount of useful light as a conventional 150-W parabolic aluminum reflector incandescent floodlamp while consuming 60 percent less energy.

It's all done with mirrors

High-resolution optical scanners are indispensable in laser printers, video data recording systems, and other technologies. The heart of most of these scanners is a rotating polygonal mirror, which repeatedly deflects a laser beam through an angle. Imaging optics focus the beam to a small spot of light to scan a line on a rotating drum or other medium. The optics also compensate for cross-scan error: displacement of the scan line caused by inevitable manufacturing errors in making each facet parallel to the polygon's axis of rotation.

Resolution can be increased by either speeding the rotation of the polygon or adding more reflective facets. But increasing the speed can introduce dynamic instability, distortion of the facets, siren noise, and excessive wear. And increasing the number of facets diminishes their size, which can impair resolution, scan field angle (maximum angle over which the beam can scan), and duty cycle. Making the polygon larger to accommodate more facets of the optimal size may not be an option if the overall product is to be compact.



At least one inventor has suggested placing close to the polygon a small flat mirror to reflect the light beam back to the same facet for extra deflections [see figure]. With each additional deflection, the scan field angle increases by the same amount as that for a single deflection, allowing the use of a polygon with many more facets than in conventional scanners.

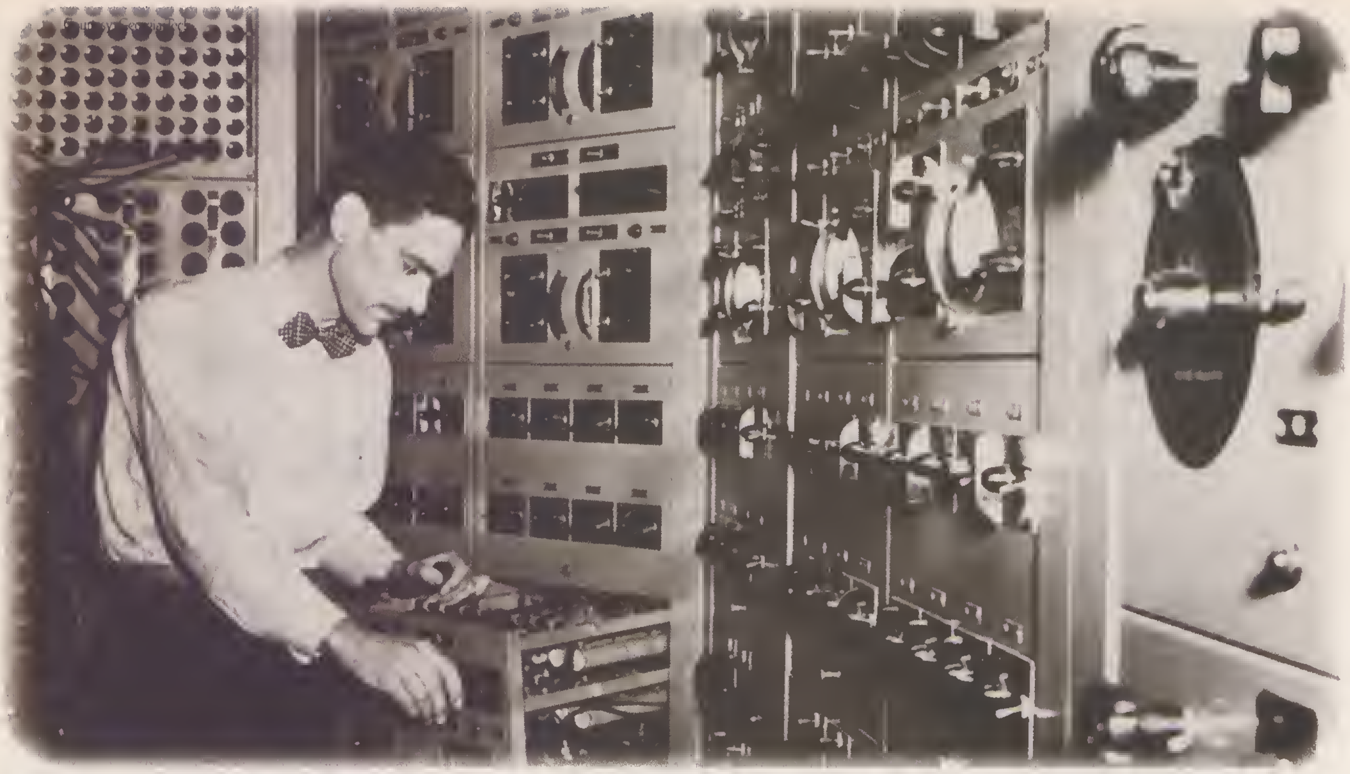
However, until recently there has been one intractable problem: the cross-scan error also increases in direct proportion to the number of deflections. Now, Mahmoud Razzaghi, an independent researcher in Lemon Grove, Calif., has developed a self-correction technique for minimizing cross-scan errors, making high-resolution optical scanners based on multiple deflection practical for the first time. He received U.S. patent 4 960 312 on Oct. 2, 1990.

In Razzaghi's system, the scanner's laser beam is first collimated, and then sent through a cylindrical lens, which causes it to converge into one flat beam perpendicular to the polygon's axis of rotation "so that it becomes like a horizontal knife edge," Razzaghi explained. This converging knife-edge beam is directed at the polygon from below the flat mirror. The beam bounces several times between a facet and the mirror, and it starts to diverge again.

If the facet is tilted away from parallelism with the flat mirror, the angle at which the beam strikes and is reflected from the mirrors widens or narrows—shifting the beam up or down the facet, thus displacing the resultant image and creating cross-scan error. But in Razzaghi's system, the beam rotates in a direction opposite to its vertical shift up or down the facet, compensating for that shift.

According to Razzaghi, his invention can allow optical scanners to have a resolution as high as 30 000 dots per line and data rates as high as 90 megabits per second.

COORDINATOR: Trudy E. Bell
CONSULTANTS: Ralph H Baer and Homer Jensen



TECH

APRIL 1991 Volume 28 Number 4

A chicken-and-egg problem

Engineers often work at the cutting edge of development but are slow to use their own developments. That may not be simply a case of the shoemaker's shoeless children.

A historic example would be television, where pioneers labored to improve resolution, sharpness, linearity, and the like. But they probably watched more test patterns than their neighbors did wrestling.

Undoubtedly their casual interest in television fare stemmed in part from the limited programming. In his 1979 biography, David Sarnoff remembered that CBS Television in 1946 "consisted of one station broadcasting six to ten hours a week."

Ultimately the gap in television programming was closed, and today, between networks and cable, at least in the United States, the viewer can choose from a range of excellent to atrocious programs.

Today we face a similar situation in the use of computers for the publication and retrieval of specialized information, of the kind that is now published by the IEEE and other professional societies in hard-copy format.

When the editors of *IEEE Spectrum* recently convened groups of readers to discuss how they obtain the necessary information to do their jobs, the aforementioned topic came in for much attention.

By and large, the participants in the groups were employed by industry or governmental agencies. Some, working on the design of computer hardware/software themselves, viewed the electronic storage and retrieval of technical information as an important new market for their own organizations to cultivate.

Yet, while almost all had personally tried to use existing information search and retrieval systems, and many had high hopes for their future success, most were disappointed in their current experiences.

Criticisms centered on the time required to search and on the failure of the searches to yield wanted information. Many saw the problem as a superabundance of literature but deficient programming that cannot converge on the few sources they needed for a particular project. One senior engineer remarked that "at this point in time you can't get a reasonable number of hits. Focusing in on the right articles is hard." A number of the participants found the systems not user friendly. One computer designer said he would not spend the hours required to learn to use a particular system. Others confirmed this, saying they go to their company librarian for help. "On three or four occasions," one said, "I have tried diligently to use computer retrieval, indices, and keyword searches, sitting with our librarian and saying, 'Let's use this or that key word,' and it does not turn out well." Another said his experience with CD ROM was that "you can miss articles that are of great interest—seminal articles and somehow they don't come up."

Some expressed impatience with the search procedure, finding it tedious to sit before a screen. A mathematician said it's not fun to read a screen, she "would rather sit comfortably with a cup of coffee and read hard copy." Another, "you can't make notes in the margin of a video screen."

Many of the papers that an engineer seeks when starting out on a new project are at the cutting edge. Some have been presented at conferences but are not yet published. Therefore, said the participants, these papers have not found their way into any electronic database or retrieval system. Transactions and journal articles, they said, with the lengthy review and publication cycles, are late enough; adding to that delay the time needed to index them and get them into a retrieval system, they said, ensures a certain obsolescence

On the other hand, researchers tend to work in a less time-sensitive environment than do design or development engineers, and they are more likely than someone up against a design deadline to put time into using a computer-based system to search the literature.

Norm Bendell

So they can find what they want when they want it, many engineers hoard too much information.

Unlike television or other consumer products, however, the solution does not lie in programming for the masses, where investments can be amortized over a huge user base. The engineer (or the architect, or the physician) wants to pinpoint a sometimes elusive answer that is embedded in a burgeoning volume of arcane information—papers, conference records, reports, and the like.

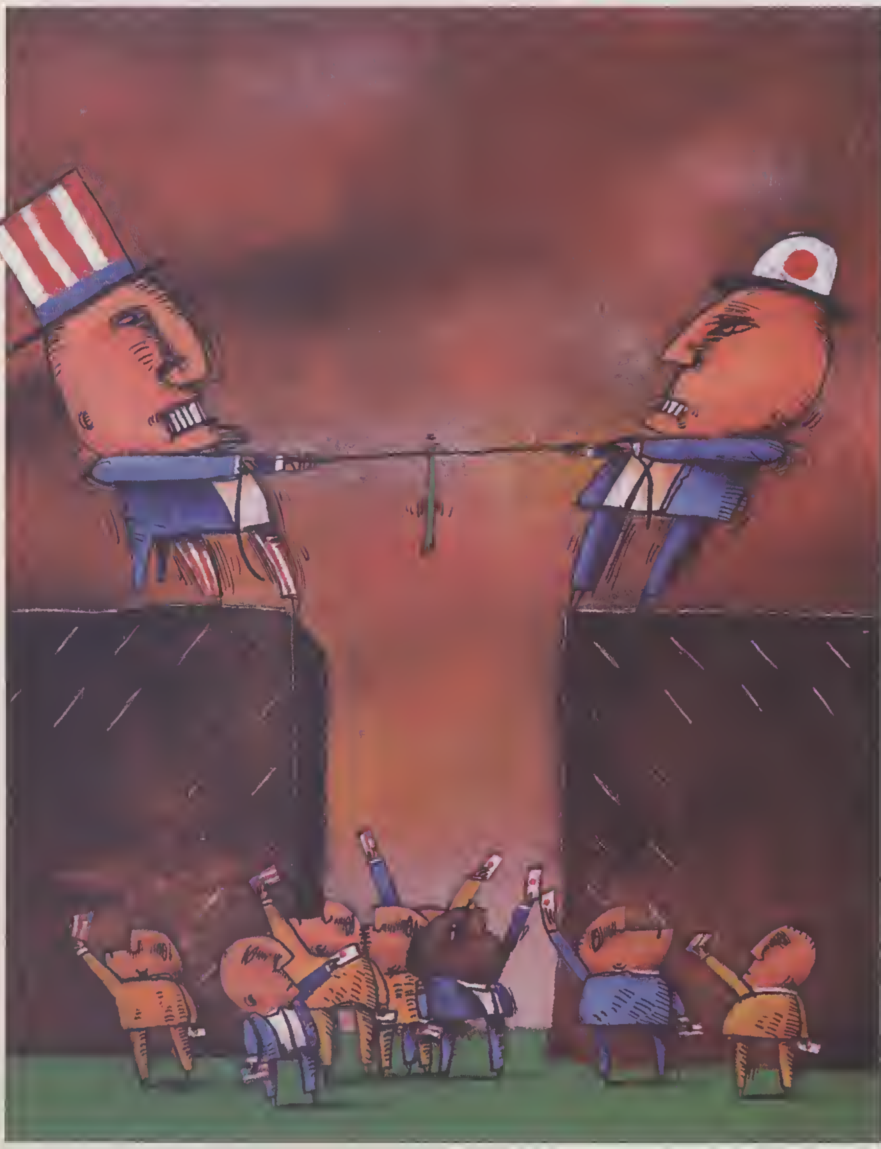
One of the responses to the current situation is that engineers tend to save what they think they may need to retrieve in the future. One told *Spectrum* that the engineer in the office below him, as she glances up warily at her ceiling, is concerned that his cache of journals and other reports is exceeding the building code's floor-loading limits.

The "scan and save" process is deemed an unnecessary burden by many engineers. Hard copy will always have its place, they say, but they'd like to be able to use the fruits of their own technologies to ease the search and retrieval process.

Donald Christiansen

WHO'S AHEAD IN HI-TECH?

Responses to Gallup survey by U.S. engineers



Illustrations by James Yang

Most sampled U.S. engineers think the United States will hold the lead through 2000, but industry observers found some of their views overoptimistic

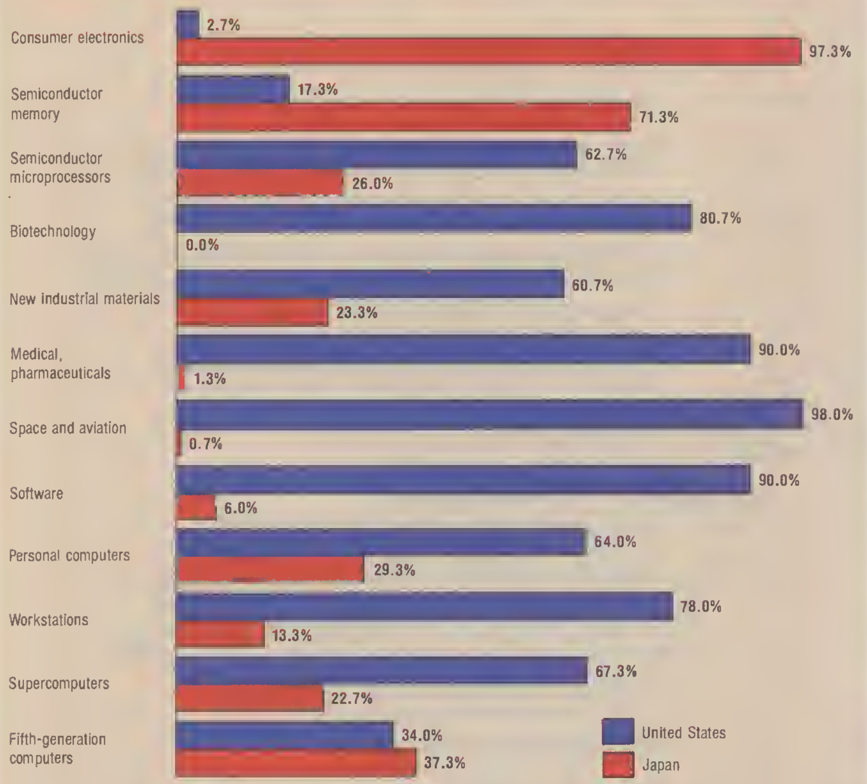
Despite talk of declining U.S. industrial competitiveness in both America's Congress and industry, U.S. engineers believe the United States holds a technological edge over Japan in many areas. The majority also believe that the U.S. lead will continue into the next century, and that the Japanese should not be credited with being technological innovators since they have been using basic technology developed in other countries.

These were among many opinions expressed by a sampling of IEEE members selected at random from the circulation list of *IEEE Spectrum* in a telephone survey conducted last fall. The survey was sponsored by *Nihon Keizai Shimbun*, a Japanese counterpart of the *Wall Street Journal* that is regarded as the largest-circulation business daily in the world.

The interviews were conducted by the Gallup Organization Inc., of Princeton, N.J., which asked 150 IEEE members—50 each from government, industrial, and academic facilities—to respond to more than two dozen questions, some of which were suggested by the IEEE. Though the sample was small, Gallup chose the respondents randomly from each category, seeking to obtain

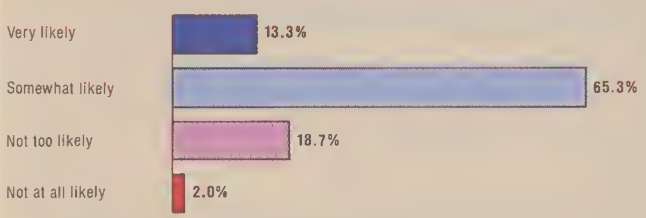
Alfred Rosenblatt Technical Editor

1. Who's ahead in technology?



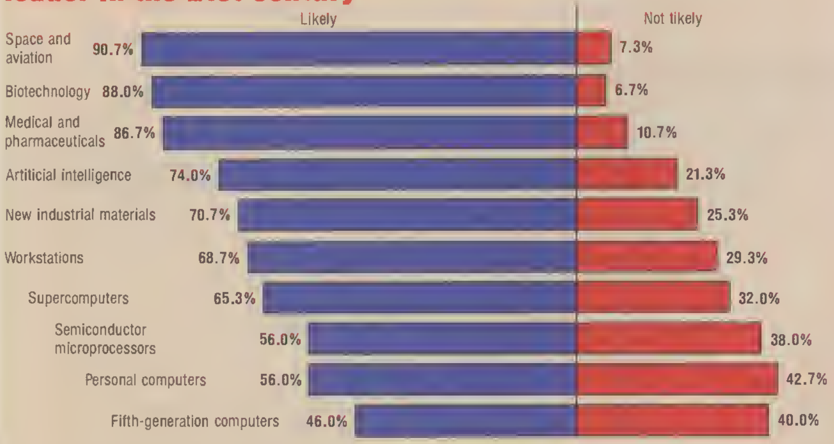
Note: Percentages of respondents who answered "don't know" or said that both countries are "equally advanced" are not shown.

2. What is the likelihood of the United States holding the technological edge in the 21st century?



Note: Percentages of respondents who answered "don't know" are not shown.

3. Areas in which the United States is likely to be a global leader in the 21st century



Note: Percentages of respondents who answered "don't know" are not shown.

a valid sampling that would tend to indicate opinions of the IEEE's U.S. membership in general.

The majority of the sample—almost 77 percent—said they were involved with electronics, electrical engineering, or computer software. Three times as many—18 percent—were engaged in software development as were engaged in computer hardware design (6 percent). Others identified their work as being in six other technical areas: energy (7.3 percent), biotechnology (3.3 percent), data processing (3.3 percent), new industrial materials (2 percent), medical or pharmaceutical research (1.3 percent), and superconductivity and environmental technology (0.7 percent each).

When asked to assess which country was furthest advanced in his or her own area of technology, almost two-thirds (65.3 percent) said the United States was dominant. About one-fifth—19.3 percent—believed the Japanese were. A tenth called it a dead heat.

That most consider the United States the leader is not necessarily at odds with the perception of a decline in U.S. competitiveness. A technological lead is not invariably the best indicator of marketplace success [see "Responding to the respondents," p. 26].

Japanese see parochialism in views of U.S. engineers

To develop the assessment in further detail, engineers were asked about 12 of the world's "hot" technical areas, ranging from consumer electronics to biotechnology to fifth-generation computers. It was scarcely a surprise that almost all—97.3 percent—believed the Japanese were ahead in consumer electronics [Fig. 1]. If there was a surprise, it was that 2.7 percent believed the United States has the lead.

Japan was also rated as the leader in semiconductor memory (71.3 percent). A minority said the United States was the leader (17.3 percent), while a handful called it another dead heat (7.3 percent). The rest said they did not know.

In addition, the Japanese just nosed out the Americans in fifth-generation computers (37.3 percent to 34 percent). This category also totaled the largest percentage of "don't knows" in the survey (21.3 percent).

But in all other categories, the United States won in a walk. The percentages ranged from almost all (98 percent), who be-

lieved the United States was dominant in space and aviation, down to a still hefty margin (62.7 percent) who put the United States ahead in semiconductor microprocessors.

Queried on the likelihood of the United States' holding the lead in these areas in the 21st century, again, a hefty portion (78.6 percent) felt that the United States would hold its technological edge (as well as, according to the question, "maintain its current level of economic power and international competitiveness") [Fig. 2]. Most (65.3 percent) said it was somewhat likely, while a minority (13.3 percent) viewed it as very likely. Another minority (18.7 percent) characterized the prospect as not too likely.

> Advice for U.S. companies: forget the not-invented-here syndrome and take keener interest in Japanese techology

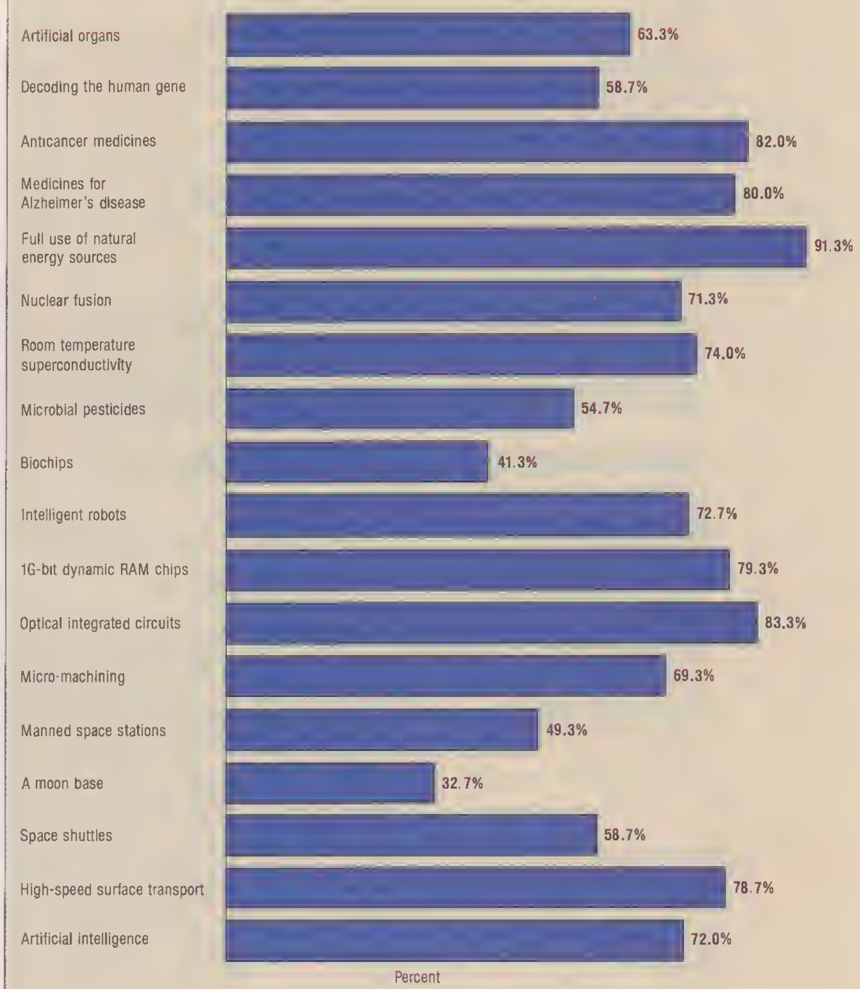
In general, though, respondents thought the U.S. lead in most areas would slip by the next century [Fig. 3]. In only two areas—biotechnology (chosen by 88 percent) and fifth-generation computers (46 percent)—did more respondents believe the United States would increase its lead.

DIFFERENT VIEW. The U.S. Department of Commerce, however, has a decidedly different view of the country's technological status. The department has warned that the United States is in danger of being surpassed by the Japanese in 11 major "emerging" areas of technology—areas it judges will be important economically by the end of this decade [see "The expanding world of R&D," *Spectrum*, October 1990, p. 28].

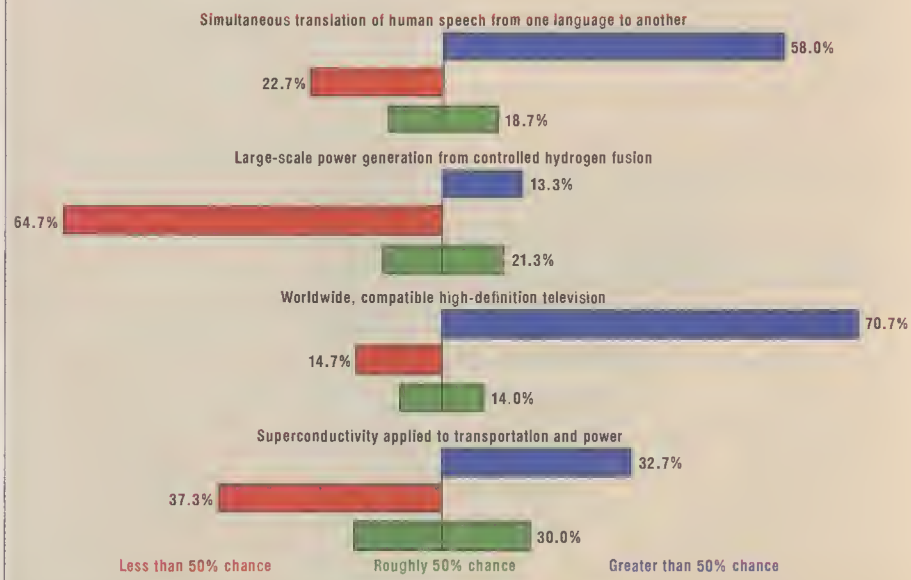
The Department of Commerce likens these new areas to the then fledgling microprocessors and semiconductor memory advances of the 1970s. Just as those technologies grew to billion-dollar industries in the 1980s, the department expects that a new group of now embryonic technologies will be mature enough to drive the world's high-tech economies by the turn of the century and beyond.

By 2000, then, if U.S. firms are successful in bringing these technologies to market at the best price, performance, and quality, it will "stimulate more and better quality

4. Where should the United States place its technological priorities?

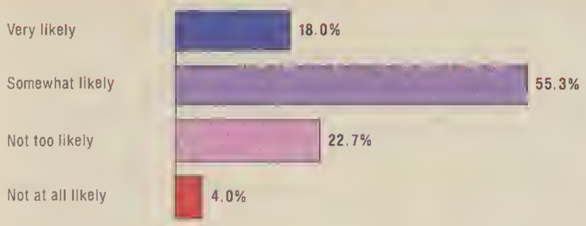


5. By 2010, what are the chances for technological advances in . . .?

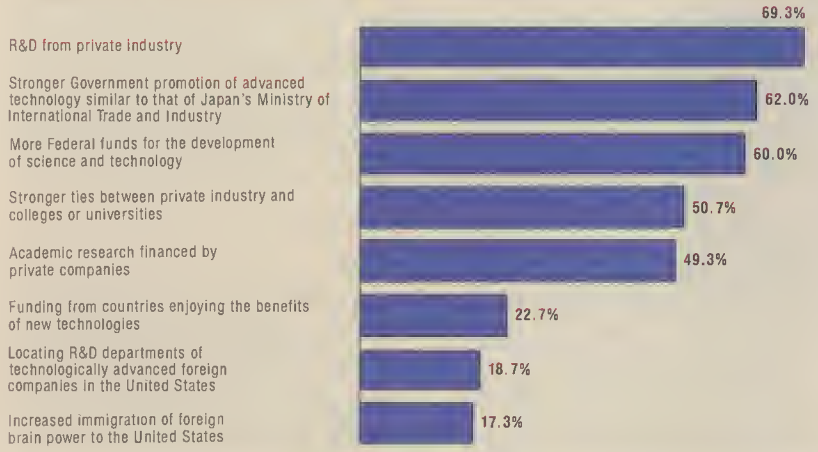


Note: Percentages of respondents who answered "don't know" are not shown.

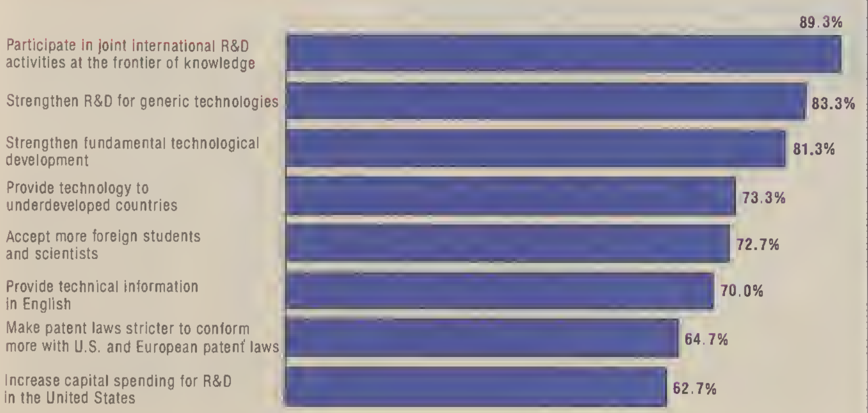
6. Is the transfer of military technologies to industrial and consumer uses likely to revitalize U.S. industry?



7. Factors promoting U.S. dominance in science and technology in the 21st century



8. Future roles for Japan



jobs, increase exports, reduce imports, and contribute directly to material wealth,'' according to a study by the Department of Commerce on the competitive status of the U.S. electronics industry.

Though the department rated the United States even with Japan or in the lead at the R&D level in those 11 areas, it put the Japanese ahead in most areas when it came to efforts to develop products.

Areas in which the department awarded the lead to the Japanese were product development involving advanced materials, advanced semiconductor devices, digital imaging, superconductivity, high-density data storage, and optoelectronics. It rated the United States and Japan even in flexible integrated manufacturing and sensor technology, and although it also rated both countries in a tie on superconductors, it said Japan is gaining.

The United States, according to the department, was ahead in three areas: artificial intelligence (where it was holding its own) and in high-performance computing systems and medical devices and diagnostics (where Japan was gaining).

CHOOSING PRIORITIES. Asked to choose where the United States should place its priorities and efforts, the respondents seemed to throw financial considerations to the wind. Fully half of the 18 technical areas listed received the vote of two-thirds or more of the respondents [Fig. 4]. Almost everyone's favorite (91.3 percent) was the ''full and effective usage of natural energy resources.'' However, the category was not precise enough to draw the distinction between the

> A minority sees transfer to civilian use of technology developed for the military as very likely to revitalize U.S. industry

use of polluting fossil fuels like coal and petroleum and such cleaner, renewable energy sources as alcohol, solar energy, wind, and water.

Next in popularity was optical integrated circuitry (83.3 percent), while medical concerns were also high. Interest in the last proved the old journalistic adage that *everyone* is interested in a good medical story.

This was the case here even though less than a handful of respondents (4.6 percent) were involved in allied areas like biotechnology or medical and pharmaceutical research. Anticancer medicines (82 percent) topped the list, closely followed by medicines for Alzheimer's disease (80 percent). Alzheimer's medicines just nosed out efforts for developing gigabit dynamic RAMs (79.3 percent).

Other areas scoring high percentages were high-speed surface transportation (78.7 percent), intelligent robots (72.7 percent), artificial intelligence (72 percent), and micromachining (69.3 percent). At the low end of the scale were a moon base (32.7 percent), biochips (41.3 percent), and manned space stations (49.3 percent).

The majority of respondents also put their faith in the ability of engineers to come up with useful solutions to some of today's tricky technological problems [Fig. 5], according to responses to several questions supplied by the IEEE for the survey. Fairly wide majorities believed that chances were "greater than 50 percent" that by the year 2010 a computer could provide virtually simultaneous translation of human speech from one language to another (58.0 percent), and that compatible high-definition television would be in operation worldwide (70.7 percent).

A significant majority, however, believed there was less than a 50:50 chance that large-scale power generation by controlled hydrogen fusion would be possible by then (64.7 percent). And the respondents were fairly evenly divided about the possibility of superconductivity being applied to transportation and power generation by that year. The largest number (37.3 percent) believed there was less than a 50 percent chance of this happening, while a slightly smaller number (32.7 percent) believed that likelihood was greater than 50 percent.

In response to another IEEE-posed question, almost all respondents (94 percent) agreed that engineers should take a more assertive role in helping the public understand the pros and cons of the introduction of technology. They "mostly" agreed with the statement that engineers should help government decision-makers and the general public "understand the costs, benefits, and risks associated with the application of various technologies."

Regarding environmental concerns, almost all respondents (95.3 percent) agreed, in answer to another question from the IEEE, that over the next 20 years "engineering and technology will have a mostly positive effect on the global environment." Here they apparently had in mind technology's being applied to make manufacturing and other processes more efficient and less wasteful, as well as its use in correcting problems of pollution. [For a discussion of several ways engineers might affect the political process in the United States, see "The politics of science," p. 15.]

Respondents also considered several factors that might be "likely" to prevent future technological advances by the United States. Heading the list was less spending for R&D by the U.S. government and private compa-

Responding to the respondents

Asked to comment on the survey results, industry observers offered some perspective as well as opinions that differed from those of the engineers responding. Jack Doyle, vice chairman of the IEEE United States Activities Committee on U.S. Competitiveness, disagreed with the 78.6 percent of respondents who believed it "very likely" or "somewhat likely" that the United States "will hold the technological edge in the 21st century and maintain its current level of economic power and international competitiveness."

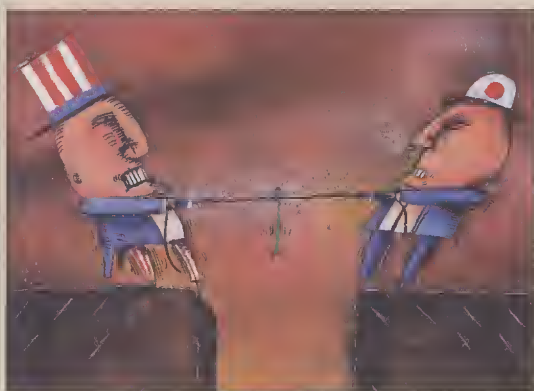
"It could very well hold the technological edge and not maintain its economic power and competitiveness," he said. "The question assumes they all go together and this is not necessarily so."

PAROCHIALISM A CONCERN. Taizo Yakushiji, a professor at the Institute for Policy Science of Saitama University in Urawa, Japan, just north of Tokyo, warned that a "parochialism" in the United States could contribute to "an even steeper decline" in U.S. technological prowess than has already been experienced. After analyzing the survey results, Yakushiji expressed his opinions of them in an article that *Nihon Keizai Shimbun* published along with its presentation of the survey.

A country's prosperity depends on its advanced technology, Yakushiji pointed out, and a country that neither learns from other countries nor wants to update its technologies "will be headed for a downfall." In his view, U.S. parochialism could lead to the country's becoming "weaker than people [responding to the survey] now believe it will."

He was also critical of respondents who felt that the most important role that Japan can play is to participate in and support joint international research efforts at the frontier of technology. "I think this means that American researchers simply want money from Japan," he wrote. "In other words, they think Japan is rich and does not have the technologies [the respondents] are interested in."

This concept of Japan's technical accomplishments, or, rather, the country's lack thereof, "indicates the degree of parochialism in the United States," Yakushiji continued. He found such thinking also reflected in what he called respondents' "Japan bashing," as well as in their negative attitude toward Japan. He felt that attitude was apparent when respondents said that Japan wants an "easy ride" and that Japanese companies only want to obtain advanced technologies and don't want anyone to learn about what they have developed.



Yakushiji also viewed with alarm the possibility that the industrialized countries might establish a "containment policy" to guard against the dissemination of information about their advanced technologies. (A large minority of respondents [36.7 percent] thought it "very" or "somewhat" likely that an embargo would be placed on "hot" technologies.)

He also cautioned that relations might worsen if Japan and the United States performed joint research but only one country then brought the research to "a successful [meaning commercial] conclusion." Yakushiji likened the hostile relationship that might develop between the two countries to that between the United States and the Soviet Union during the Cold War.

Just as those two antagonists promoted détente in order to survive, so would the United States and Japan. The two "will have to seek a way to improve the hostile relationship; otherwise, both countries will be on the way to a downfall," he concluded.

Michiyuki Uenohara, executive advisor of NEC Corp., Tokyo, found the responses reflected a general U.S. point of view about Japanese capabilities. "If the poll were directed to specialists who have [a] good knowledge of current Japanese R&D. . ., the response could have been considerably different," Uenohara said.

He said he was "very much surprised" that 62 percent of respondents believed that Japan is having an "easy ride" on basic technology developments from other countries. "Don't they know that Japanese contribute so many papers to IEEE transactions and international conferences?" he asked. "Do they still think that basic technology is created only by Nobel Prize winners?"

NO MORE NIH. U.S. companies should take a keener interest in Japanese technology, and should give up the not-invented-here syndrome, Uenohara continued. He added that a great deal of technical information available from Japan is printed in English.

Bruno W. Weinschel, former IEEE President and president of Weinschel Research Foundation, Gaithersburg, Md., pointed out that basic work in Japan is done not in universities, as it is in the

nies (each with about 89 percent). A decline in educational level was another consideration, as was a shortage in the number of scientists, researchers, and engineers (each with about 79 percent).

Also cited was a decline in the U.S. gross national product (74.0 percent), and almost two-thirds were concerned that economic or trade conflicts, as well as an increase in protectionism, might prove "likely" to bar such advances. Somewhat fewer (62 percent) thought that negative public attitudes might come into play. Going down the scale, less influential factors were wars or conflicts between countries (48 percent), running out of natural resources (44.7 percent), and natural disasters (30.7 percent).

MILITARY CUTS. If the military budget were to decrease by 10 percent over the next five years, exactly half the respondents felt that technical development in the United States would decrease by only a "modest" amount. However, the Bush administration has called for a 25 percent decrease in military funding. This large a decrease might cause more than a modest concern. A minority of some size (18.7 percent) said that military R&D does not lead to technological advantage. According to them, a decrease in military R&D would lead to an *increase* in technological development on the assumption, perhaps, that the R&D money would be well spent elsewhere.

In another area of interest to the Bush administration—the transfer of technology developed for the military to civilian use—a majority (55.3 percent) felt that such efforts would be only "somewhat likely" to revitalize American industry [Fig. 6]. A minority (18 percent) thought it "very likely" to revitalize it.

The majority view Japan as having an easy ride on technology developed elsewhere

In selecting factors that would enable the United States to maintain its position as the "dominant global power" in science and technology in the next century, more than two-thirds of respondents (69.3 percent) judged that funding for R&D from private industry would be the most important factor [Fig.7]. It should be noted that in the last fiscal year, funding for R&D in the United States—at roughly US $150 billion—was judged to be divided about equally—between government and industry, according to a National Science Foundation estimate.

A large majority (62.0 percent) also believed that global dominance could be assured by stronger Federal government funding of advanced technologies in a manner similar to the efforts of Japan's Ministry of International Trade and Industry. Another important factor was felt to be stronger ties between private industry and colleges or universities (called for by more than half of the respondents); about an equal number stressed the importance of academic research financed by private companies. Less than a quarter felt that R&D efforts by foreign companies in the United States or taking advantage of emigres' brain power would be important in keeping the United States a global leader.

More than half (54 percent) seemed to look back fondly at the accomplishments of large-scale Government-sponsored projects, like the Manhattan Project and the Apollo space program. Similar commitments, respondents indicated, would be needed for the United States to make progress in technical developments.

AN EASY RIDE. The idea that Japan may have by now produced its share of technological innovators and original thinkers seemed not to have penetrated the respondents. A large majority (62 percent) said Japan is having an "easy ride" on "basic technology developed in other countries."

Along similar lines, a large number (74.7 percent) agreed with the assessment that "Japanese companies take a lot of technology from the U.S. but provide very little technology to American companies in return."

A sizeable minority also seemed concerned that Japan's "easy ride," and its perceived borrowing of ideas without providing anything in return, might lead to ill will between Japan and the United States. This was suggested by the supposition that an embargo would be placed on "hot" technologies by the United States, Japan, or the Europeans in the near future. They believed it "very likely" or "somewhat likely" that this would occur (36.7 percent). However, the majority believed it "not too likely" or "not at all likely" (57.4 percent). Another majority (68.7 percent) indicated it would be "mostly good" for American technological competitiveness if Japanese companies continued to increase the number of research laboratories they are setting up in the United States.

However, some dissenters (22 percent) indicated this would be "mostly bad." Even more (30.7 percent) indicated they would not be interested in working for a Japanese R&D facility in the United States; more than half (58 percent) indicated they were interested.

More than a third (35.3 percent) said they would like to work at a research facility in Japan. Cited most often as the reasons for this decision were the chance to travel, to live abroad, and to get to know another society.

In what is very likely typical of the experience of most U.S. engineers, respondents reported having had very little direct contact with Japanese companies or engineers. Most (82.7 percent) said they had never worked on a joint research or development project with a Japanese company. And only a handful (7.3 percent) indicated that they had plans for a joint R&D project with the Japanese, although most (74.7 percent) said they would like to set one up.

Even though most respondents did not credit the Japanese as being basic innovators or creative thinkers, a majority felt that Japan could play many important roles because of its position as a technologically and economically advanced country [Fig. 8]. They indicated they wanted the Japanese to do such things as participate in joint international R&D activities at the "frontier of R&D" (89.3 percent) and increase capital spending for R&D in the United States (62.7 percent). ◆

United States, but in corporate laboratories which do not necessarily publish the results. "In the United States, academia must publish or perish," he said. "We are not getting important information from Japan because of its source control, particularly in practical subjects like manufacturing processes, tool design, and materials."

Weinschel also felt it was wrong to assume, as respondents did, that the United States was ahead in bioengineering. "Japan has excellent fermentation industries, one of the infrastructures needed for the quick application of bioengineering," he said and urged greater U.S. efforts in this area.

POISED FOR SUCCESS. But another respondent put the case even more strongly. "Japan is poised to be strong in biotechnology," said Mark Dibner, director of the Biotechnology Information Division at the North Carolina Biotechnology Center, Research Triangle Park, N.C. He agreed with respondents' estimation that the United States currently holds the lead, but he felt the question should really ask, "The lead in what?"

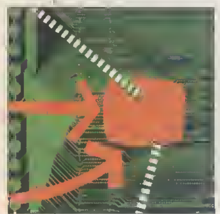
In his opinion, the United States leads in basic research and in early product development. "We are good, but we are also good at giving away the technology for a fraction of its worth, just as we have done with some areas of electronics," he said.

In a study Dibner made recently of biotechnology efforts in Japan, he noted that "manager after manager told me that they look to the United States as a source of technology." He also pointed out that very few U.S. consumers are aware of biotech products; the Japanese consumer is much more aware.

"The Japanese know they wash their clothes in bio-detergents or can buy bio-wines or bio-lipsticks," he said, adding that this is another reason why the Japanese are poised to be strong in the field. *—Alfred Rosenblatt*

The challenges of digital HDTV

Complex compression coding and motion compensation algorithms are key techniques used by system designers



In a sudden series of masterstrokes, U.S. engineers have propelled high-definition television (HDTV) into the digital era. Until last June no all-digital HDTV systems were candidates for a terrestrial HDTV broadcasting standard in the United States. Now four are scheduled to be tested by the Federal Communications Commission (FCC).

The move to digital began in June when General Instrument Corp. announced its DigiCipher all-digital system. In November, the Advanced Television Research Consortium—National Broadcasting Co. (NBC), David Sarnoff Research Center, Philips Consumer Electronics Co., and Thomson Consumer Electronics Inc.—gave notice that a digital system would be developed jointly by the Sarnoff Center and Philips Laboratories.

In December, Zenith Electronics Corp., AT&T Bell Laboratories, and AT&T Microelectronics announced their joint development of an all-digital system (Zenith's previous entry had been a hybrid analog-digital design). And in January, General Instrument was again in the news with the revelation that it had joined with the Massachusetts Institute of Technology (MIT) to form the American Television Alliance, which would submit two systems for testing: the DigiCipher system and a system to be developed with MIT.

WHY DIGITAL? Back in March 1990, the FCC announced that it would consider only simulcast systems for a U.S. terrestrial broadcasting standard—systems where one broadcast channel carries a standard National Television System Committee (NTSC) signal for reception on existing television receivers, and a second channel carries the HDTV signal for reception on HDTV sets. But FCC chairman Al Sikes made it clear that the door was being left open for any new technological developments that might arise.

Ronald K. Jurgen Senior Editor

Sikes said: "...the Commission wishes to review carefully but quickly in early 1992 any...new advanced television developments. If in the course of that examination the Commission finds that a new advanced television technology is sufficiently concrete and developed to the point that it can be tested, the Commission will supplement the testing procedures and timetable to accommodate it." He gave as an example the development of a fully digital system.

But over and above whatever the FCC may have intended, digital HDTV offers certain advantages over an analog or hybrid system. First and foremost, a broadcast digital signal should in theory supply home HDTV receivers with pictures that are free from atmospheric noise, let alone interference from motors, car ignition systems, citizens band radios, and the like.

According to James E. Carnes, head of the David Sarnoff Research Center, digital HDTV has additional advantages. The very sophisticated compression techniques that can be implemented digitally should produce superior image resolution and sharpness; and a digital approach provides more flexibility for channel utilization or to meet new scanning standards in the future.

"Fulfilling the digital promise, however, is no easy task," Carnes told those attending the IEEE Media Briefing in New York City in November. Any simulcast signal must peacefully coexist with a rather hostile NTSC broadcast environment. The digital signals must not interfere with or degrade existing NTSC channels. Further, the digital signals have to be resistant to interference from existing high-power NTSC signals.

Digital service also naturally tends to degrade abruptly. Unlike NTSC pictures, which deteriorate slowly as distance from the transmitter increases, but are still watchable, pictures from digital transmissions simply vanish. For example, one home receiver might get an excellent picture and the receiver just down the block, a little farther away from the transmitter, might get nothing, Carnes said.

The biggest issue for digital transmission in the terrestrial broadcast environment is how large the coverage area will be, Carnes told *IEEE Spectrum*. Since spectrum is limited to the present very high-frequency (VHF) and ultrahigh-frequency (UHF) channels, currently unused channels must be harnessed for simulcast signals. Since these signals cannot significantly degrade existing NTSC service, the transmitter power must be limited—especially in heavily populated areas where spectrum is crowded. The issue, then, is whether the resultant coverage area will be large enough to make good business sense.

Despite these formidable challenges, all the system proponents plan to have their digital systems ready for testing in accordance with the schedule set by the FCC's Advisory Committee on Advanced Television Service, together with the Advanced Television Test Center, Alexandria, Va. That schedule calls for a September start to the testing of the DigiCipher system from San Diego, Calif.-based General Instrument; an October start for the system from Zenith, Glenview, Ill., and two AT&T units in New Jersey (the Murray Hill laboratories plus AT&T Microelectronics in Berkeley

> One home receiver might get an excellent picture and the receiver next door might get nothing

Defining Terms

Aspect ratio: the ratio of frame width to frame height as defined by the active picture.

Chrominance: the colorimetric difference between any color and a reference color of an equal luminance and a specified chromaticity.

Interlaced scanning: a process in which half the horizontal scan lines—every other one—of a television picture are transmitted first, and then the other half are transmitted and woven between the first set of lines.

Luminance: the luminance intensity of a surface in a given direction per unit of projected area.

Progressive (sequential) scanning: a process in which the entire picture is transmitted at once.

Quantization: a process in which the continuous range of values of an input signal is divided into nonoverlapping subranges, and to each subrange a discrete value of the output is uniquely assigned.

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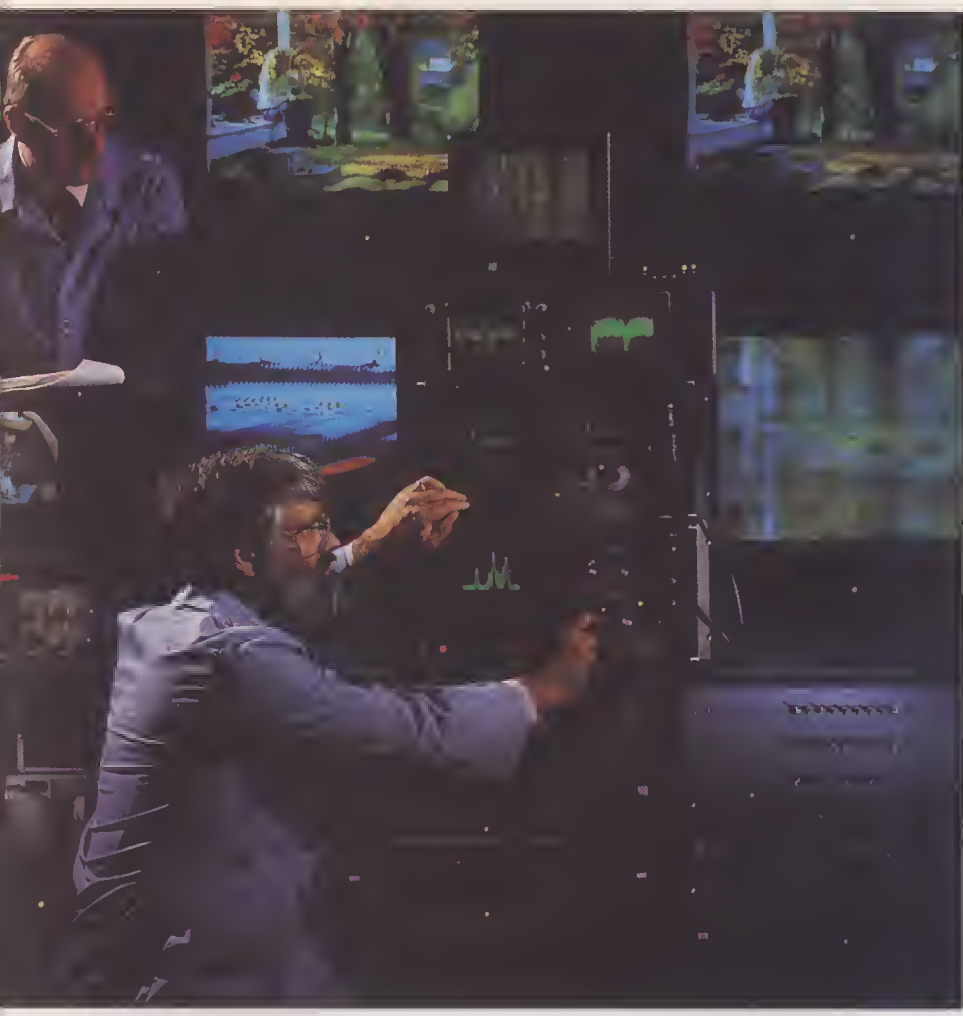


Zenith Electronics Corp.

Wayne C. Luplow, executive director of advanced research and development at Zenith Electronics Corp. (standing left), and Richard Citta, manager of electronic systems R&D, evaluate the Glenview, Ill., company's low-power, interference-free HDTV system that uses taboo channels (top row of monitors). Conventional television broadcasts using the taboo channels cause interference (bottom row of monitors).

Heights); a January beginning for the system from the Sarnoff center and Philips Laboratories, Briarcliff, N.Y.; and the following March for the systems from General Instrument and MIT in Cambridge. Until those systems are tested in Alexandria, Va., and at least one is subsequently tested in the field, no one can be sure how successfully the challenges can be overcome.

Two other systems will also be tested: an enhanced compatible system from the Advanced Television Research Consortium and an analog simulcast system from Japan Broadcasting Corp. (NHK), Tokyo. The Sarnoff ACTV system would improve existing NTSC transmissions to provide a picture with an aspect ratio of 16:9, so it is not in competition with the four digital simulcast HDTV systems. The NHK approach, however, is a competitor for a U.S. simulcast standard but, at this writing, there had been no announcement that it would be converted to an all-digital system.

SYSTEM SIMILARITIES. All four proposed digital HDTV systems have many design features in common. Besides transmitting digitally in a simulcast mode, they depend on the use of so-called taboo VHF or UHF channels.

For the simulcast approach to be widely used, every existing television broadcaster—and there are now over 1400—must have a second 6-megahertz channel in the existing television bands. No "new" spectrum will be available, so simulcast signals must be able to use the currently unoccupied and unavailable taboo channels.

Theoretically, all channels could be occupied if tuner performance was adequate, but in the interests of affordability, the FCC relaxed the requirements on tuner design by leaving channels vacant.

The taboo channels are those not presently used for NTSC broadcasts because their nearness to other assigned channels in a specific locality would cause interference. With UHF channels, for example, the minimum separation allowed by the FCC between co-channel transmitters (those with the same channel allocation) varies between 250 and 355 kilometers (155–220 miles), depending on geographical location. For adjacent channels, the minimum specified distance is 90 km (55 miles). Minimum distances are also required between channel transmitters to avoid interference from sound images, picture images, local oscillators, intermediate frequency beat, and intermodulation. Those distances may be as little as 32 km (20 miles).

The four digital-system proponents are advocating use of the taboo channels because it can take far less power to transmit carrier-suppressed digital signals than to transmit analog signals. The required average transmitted power for the digital portion of an HDTV signal can be less than 10 percent of that required by an NTSC transmitter with the same service area. Reducing the power of the digital signal, however, makes it more susceptible to interference from the much stronger NTSC signals on the same or other channels.

All proposed digital systems—as well as analog systems—also use some form of video bandwidth compression after basic analog-to-digital conversion [see "Analog in, digital out," p. 71]. These include interlace scanning, removal of source redundancy, utilizing human perception limitations, three-dimensional processing (the third dimension is time), and entropy coding.

According to Kerns Powers, a television consultant in Princeton, N.J., although interlace scanning gives a 2:1 reduction factor in the total compression, a growing body of engineers feel that interlace is a poor method for 2:1 compression as compared, for example, with diagonal prefiltering and diagonal subsampling.

Video bandwidth compression invariably involves compromises. For example, one compression technique is to transmit some of the detail in a picture over a longer period of time. If motion is taking place in the scene, however, this approach causes smearing and ragged edges of that portion of the picture in motion. So some form of motion compensation must be used to offset that effect.

All systems also use some form of error correction coding so that the digital signal input to the source decoder portion of HDTV receivers will be accurate. With video bandwidth compression, a single error—a 0 for a 1 or vice versa—can cause havoc.

A BIT MUCH. There are two reasons why digital HDTV signals occupy—before video compression—much wider bandwidths than do conventional NTSC broadcast signals.

The first reason, which also applies to analog HDTV signals, is that an HDTV image has about twice as much luminance definition both horizontally and vertically (four times as many luminance picture elements or pixels) as do conventional television systems, and further additional pixels are needed for the wider screen (16:9 aspect ratio instead of 4:3). This increase in luminance detail requires about five times the video bandwidth of conventional television systems. Since extra bandwidth is needed for

the separate transmission of the color values, or chrominance, the total bandwidth required is six to eight times that of conventional systems.

As the baseband of NTSC video for VHF and UHF channels is 4.2 MHz wide, six times that is 25.2 MHz and eight times is 33.6 MHz. So to handle the increased luminance detail and chrominance information in HDTV signals, additional channel space of 21.0–29.4 MHz is needed—in other words, the space occupied by four to five additional 6-MHz channels.

The second reason is that when the analog output from an HDTV studio camera—one luminance and two chrominance signals—is converted into a digital output, the analog luminance and chrominance signals are sampled at high rates, about 120 megasamples per second. Then the sampled values are quantized or converted into digital sample words of 8 bits, for a total of 8 × 120 or nearly 1 gigabit per second before compression.

The HDTV signal's resolution determines the bandwidth required, which in turn determines the minimum sampling frequency—twice the bandwidth, or Nyquist rate.

CODING OPTIONS. Because bandwidths occupied by digital signals are much too wide to be practical, given that the FCC has specified no new spectrum space for such HDTV signals, a variety of techniques has been devised to compress them.

The basic compression codes [see table] are outlined in the book *Digital Pictures* by Arun N. Netravali and Barry G. Haskell [see To probe further]. A practical coding system might be a combination of some of these basic codes.

One code—pulse code modulation—is described in "Analog in, digital out," p. 71. Predictive coding—differential pulse code modulation (DPCM)—relies on predicting the value of the pixel to be encoded. The encoded values of the previously transmitted pixels are used for the prediction, and only the prediction error or differential signal is quantized for transmission.

Predictive coding becomes adaptive if the prediction is based on local picture statistics, if the quantizer is "coarser" in visual terms, or if the prediction error is not transmitted whenever it is below a certain threshold. Predictive coding involves a delay in encoding a pixel until the trend of the signal can be more accurately observed and then coded accordingly.

In transform coding, blocks of intensities of pixels are linearly transformed into blocks of frequency data called coefficients. Selected coefficients are then quantized for transmission. Adaptive transform coding is done in one of two ways: by changing the transformation to match picture statistics, or by changing the criteria for selecting and quantizing the coefficients to match the subjective quality requirements.

Digital signals can be transmitted with far less power than that needed for analog signals

Interpolative and extrapolative coding techniques send a subset of the pixels, and the pixels in this subset are then extrapolated or interpolated in the receiver to obtain the untransmitted pixels. Adaptive coding involves varying the criteria for selection of the samples to be sent and also varying the strategy for interpolating or extrapolating the remaining samples.

Statistical coding techniques are used to assign bits to the quantizer outputs of DPCM or transform coded signals to minimize the average bit rate.

MOTION COMPENSATION. Since bandwidth compression smears the portions of a picture in motion and makes their edges ragged, as noted earlier, some form of motion-compensated prediction must be used.

Motion compensation can be performed on either luminance or chrominance components or both. It is simpler to estimate motion from just luminance and then use the same estimate for chrominance. But as with bandwidth compression, a variety of techniques can be used.

Motion estimation algorithms may focus primarily on extracting three-dimensional motion parameters from a sequence of two-dimensional images. Alternatively, they may estimate velocities on a point-by-point or region-by-region basis without considering the overall motion.

ERROR CORRECTION. To minimize the effects of inaccurate digital transmissions, methods have been developed to conceal or correct the errors. These techniques often entail adding from 1 to 4 bits to an 8-bit word. The word plus its extra bits is called a block. When an error is detected in the word, the decoder in the receiver deletes the word and forms another in its place by interpolation from the preceding and/or following words. A word representing a picture element can be repeated to fill the gap formed by the deleted word. Alternatively, the preceding and following words can be averaged.

In fixed-bandwidth channels like those for terrestrial broadcasting, bits used for error correction are taken from bits available for data transmission.

More elaborate error correction is needed if several successive bits in a word are lost or changed. One approach uses a forward error correction (FEC) code such as the Bose, Chaudhuri, or Hocquenghem (BCH) code. One FEC code can correct as many as four bit errors in a 12-bit block through use of word storage from which predictions are made about words not yet transmitted.

QUADRATURE MODULATION. A method that fits two distinct signals into the same frequency space is quadrature (90 degrees out of phase) modulation. This technique has been used, for example, in the NTSC system.

The NTSC color subcarrier is chosen to be an odd multiple of one-half the line frequency so that the subcarrier spectrum interleaves with the baseband luminance spectrum. The subcarrier is then quadrature-modulated by two independent color difference signals, which together with the decoded luminance signal permit deriving the three color components: red, green, and blue. The spectral interleaving minimizes the luminance-chrominance crosstalk, whereas the quadrature modulation separates the two chrominance components.

Some techniques described are in all four proposed digital HDTV systems.

DIGICIPHER SYSTEM. General Instrument's DigiCipher system uses 1050-line interlaced scanning at a 59.94 field rate and a 16:9 as-

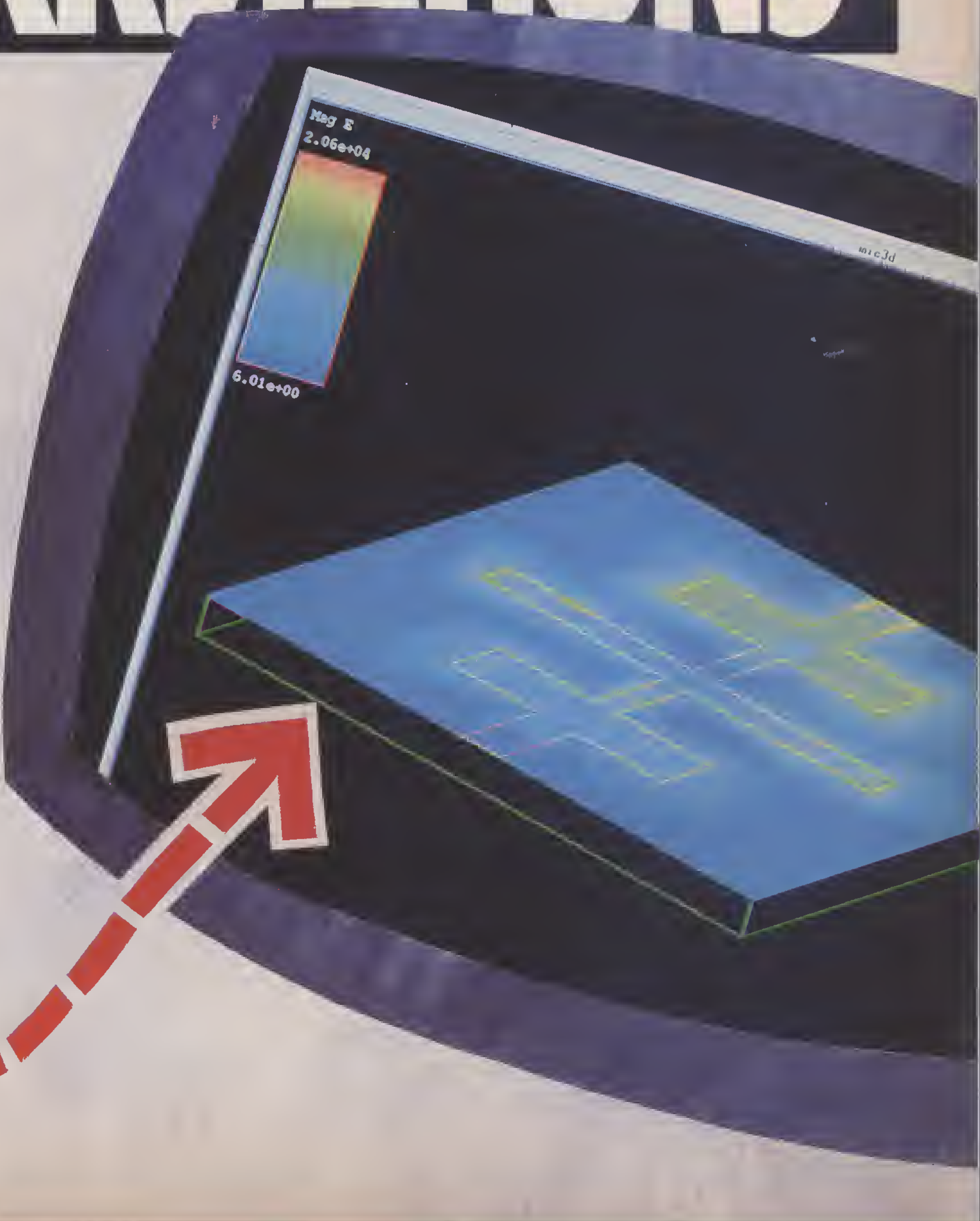
(Continued on p. 71)

Classification of picture-coding techniques

Pulse code modulation		Predictive		Transform		Interpolative and extrapolative	Statistical		Others
Fixed	Adaptive	Fixed	Adaptive	Fixed	Adaptive		Fixed	Adaptive	
			Prediction	Karhunen-Loeve	Transformation	Subsampling spatial and temporal	Huffman		Vector quantization
			Quantization	Hadamard	Coefficient selection	Adaptive	Shannon-Fano		Contour
			Conditional replenishment	Discrete cosine	Quantization		Arithmetic		Run length
			Delayed (tree)						Bit plane

IEEE
SPECTRUM

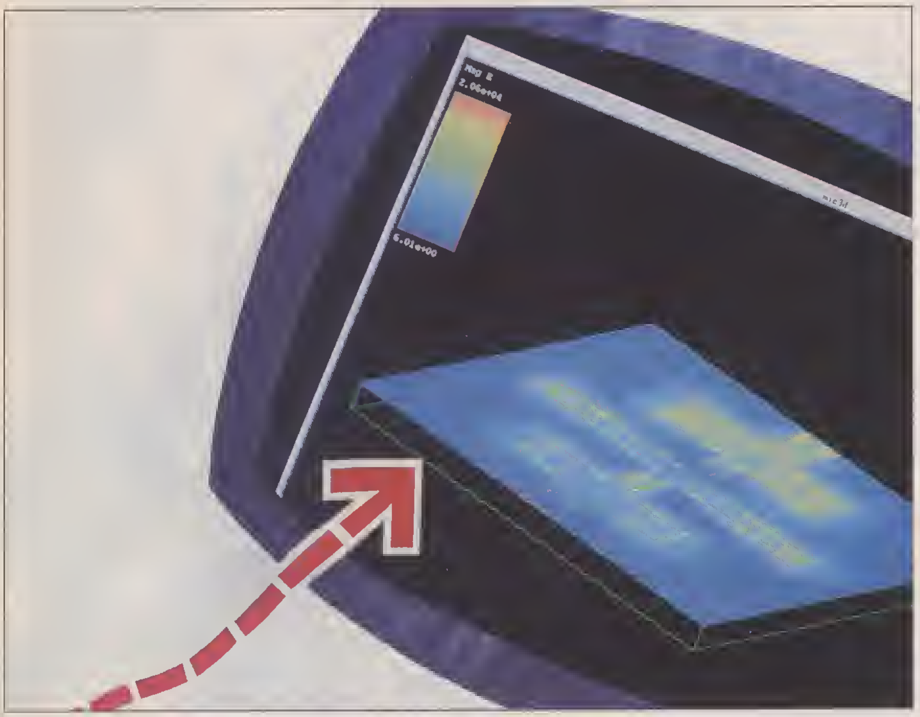
A GUIDE TO ENGINEERING WORKSTATIONS



COVERING:

- SYSTEM ARCHITECTURES
- NETWORKS AND SERVERS
- ADD-IN BOARDS
- HIGH-QUALITY GRAPHIC DISPLAYS
- MEMORY AND OTHER PERIPHERALS
- ADVANCED WORKSTATION ICs

Revolution in the workplace



Engineering is in the midst of a revolution, in which the workstation is usurping the role of most essential tool. More and more engineers and engineering managers are turning to these systems to increase the efficiency of the design process and reduce time to market. Fueling this revolution are major technological advances in computer architectures, design practices, and microelectronics price/performance ratios. And it is a self-perpetuating revolution, because the new design tools will be used to design even newer tools.

The breadth of this revolution is evident in figures gathered by Dataquest Inc., a high-technology market research firm in San Jose, Calif. According to the firm, the worldwide market for workstations exploded from nearly US $950 million in 1985 to more than $7300 million in 1990, more than a sevenfold increase in five years. That figure is even more impressive when it is recalled that the average unit price has been steadily dropping. And Dataquest's definition of a workstation is not as broad as the one *IEEE Spectrum* is using. We include under the workstation banner not only those machines that, like a Sparcstation or RS6000, have the latest reduced-instruction-set architecture; but also the high-end personal computers—those with 80386 or 68030 chips, or better. Our criterion is simple: an engineering workstation is any computer an individual can conveniently use for engineering work. Last November's software report convinced us that PCs certainly fit that definition—and Compaq Computer Corp., Houston, Texas, known for its PC-compatibles, is pushing the industry to develop a clear standard for the next generation of desktop workstations.

Gadi Kaplan Senior Technical Editor

Despite their growing numbers, workstations are far from being known quantities in every design department. And, since workstation technology changes so rapidly, users of yesterday's machines may not be familiar with today's upgrades. So both potential user and old workstation hands alike will find something to mull over in this special guide to workstation hardware. The guide combines staff-written articles and those by workstation specialists, with tables based on information collected in a recent *IEEE Spectrum* survey.

Because ergonomic considerations, which play an important part in efficient workstation operation, are often overlooked, the opening feature is a two-page illustration of what *Spectrum* considers the ideal working environment for an individual.

Yet separate workstation "islands" will not help engineers compete in technology driven markets. Today, teamwork and concurrent engineering are the important organizational issues, so workstations must be tied together into networks that optimize the use of shared resources. This is the focus of the guide's first article, "Using workstations efficiently," p. 38, from Grumman Corp., Bethpage, N.Y.

For such large companies, a distributed computing environment, in which scores of engineers exchange design information in real time, is absolutely vital. Eventually, Grumman's installation will include more than 400 networked workstations from such manufacturers as Digital Equipment, Hewlett-Packard, IBM, and Sun Microsystems.

Accompanying the article is a table listing a representative sample of workstations from over 40 companies. Because of the vastness of offerings, for this and the other tables in the guide, *Spectrum* was compelled to ask each vendor for only one of the company's most advanced products.

Even with that limitation, the table accompanying the next article ["Add-ons for your workstation," p. 52] covers four pages. That's because there are so many things that can be done to customize workstations to an individual user's needs (and because engineering demand is getting so large). Improvements are found in all areas, from ergonomic advances in the all-important input devices, such as keyboards and mice, to graphics adapters that increase resolution capabilities, memory systems that enlarge storage, and hardware accelerators that improve application performance.

The essential choice for engineers is still the basic workstation and, in order to make informed decisions, a potential purchaser should understand the way in which workstations work. In the last article in the guide ["How ICs impact workstations," p. 58], readers can gain this understanding through the eyes of a top group of engineers from Hewlett-Packard Co., Palo Alto, Calif., following their price/performance decision process as they create one of the more impressive workstations being readied for the market. (As we go to press, HP is preparing to announce a new line of workstations—the Series 700—based on this design.) Other possible IC choices are presented in a table accompanying this article. ◆

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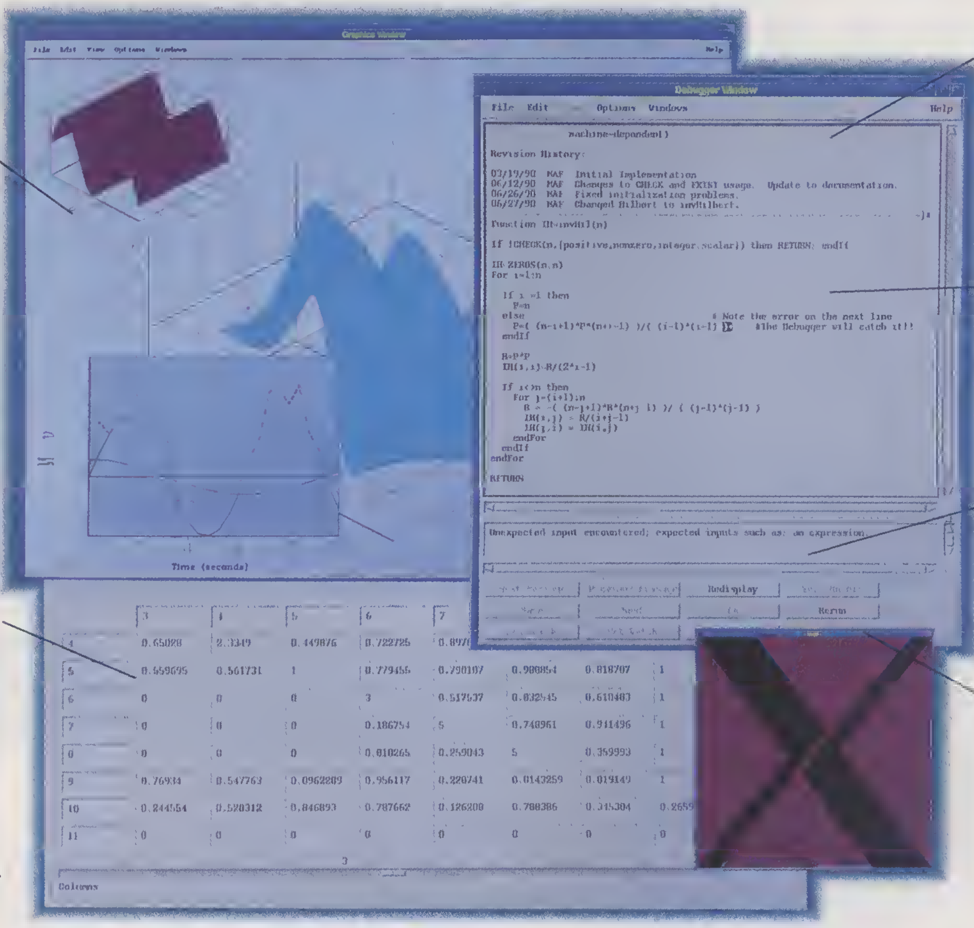
Fast Computation + WYSIWYG Graphics + Programming + Debugger + X-Windows

When you add it all up



Fast 2-D and 3-D Graphics
- ✔ *Strip charts*
- ✔ *Multiple curves*
- ✔ *Postscript, EPS, HPGL output*
- ✔ *Extensive annotation*
- ✔ *Zoom, pan, move, rotate*
- ✔ *Perspective, light source*

Matrix Spreadsheet
- ✔ *Edit matrices*
- ✔ *Cell by cell operations*
- ✔ *Access math functions*
- ✔ *Scrollable window*
- ✔ *Cut, copy, paste data sets*

Object-Oriented Mathematics
- ✔ *Algorithms optimized for data types*
- ✔ *3-D matrices*
- ✔ *Strings, tables, lists*
- ✔ *200+ built-in math functions*

Open Architecture
- ✔ *Include your C or Fortran*
- ✔ *Import your data*
- ✔ *Use ISI's MathScript to add functions*

Interactive Script Debugger
- ✔ *Source level debugger*
- ✔ *Single step*
- ✔ *Break points*
- ✔ *Variable watch*

X-Windows User Interface
- ✔ *Industry standard*
- ✔ *Pull-down menus*
- ✔ *Hypertext HELP*
- ✔ *Mouse clicks*
- ✔ *Pop-up forms*
- ✔ *Multiple windows*
- ✔ *Data dictionary*

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Xmath was designed to let you develop your own function libraries. With the built-in MathScript™ language, you can develop and debug numerical algorithms 10 to 100 times faster than with Fortran or C. The object-oriented nature of MathScript lets you capture 100's of lines of Fortran in a single command! And the friendly Motif user interface allows you to work with Xmath through pull-down menus, pop-up forms, and mouse clicks. Advanced function libraries written in MathScript are available for control design and signal processing.

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	21 Montreal, QUE	15 Los Angeles, CA

Circle No. 201

Integrated Systems, Inc. is ranked #21 in Forbes Magazine's November 1990 list of "The 200 Best Small Companies in America."

Defining terms

Cache: a high-speed memory, logically residing between a central processing unit (CPU) and main memory, that holds data the CPU is most likely to need for upcoming operations.

Cache miss rate: the number of times that an operand needed by the CPU is not found in cache memory and therefore a measure of cache algorithm performance.

Complex-instruction-set computer (CISC): a computer whose CPU is designed to run a large number of often lengthy built-in instructions that support higher-level languages. (See also reduced-instruction-set computer.)

Direct-access storage device: an electronic system for storing data online.

Error detection and correction (EDC): a process by which data stored in memory is first given a digital tag derived from that data. When retrieved, the tag is used to check the data and to correct it if necessary and possible.

Extended Industry Standard Architecture (EISA): an extension for 80386 and later processors of the ISA bus for PC-compatible computers that provides compatibility with earlier ISA systems. (See also Industry Standard Architecture.)

Fiber Distributed Data Interface (FDDI): a network based on the use of optical-fiber cable to transmit data in non-return-to-zero, invert-on-1s (NRZI) format at data rates of 100 megabits per second.

Flex circuits: circuits designed using a substrate material that is extremely flexible, typically capable of 180 degree bends.

Forward annotation: the ability to make changes in an existing design that will automatically be passed along to other operations such as simulation and automated manufacturing.

Industry Standard Architecture (ISA): the name given to the bus architecture developed by IBM Corp. for the AT version of its personal computer. (See also Extended Industry Standard Architecture.)

Latency: the time between the completion of the interpretation of an address and the beginning of the actual transfer of data from the addressed location.

Physical address: a binary address that refers to the actual location of information stored in a second level of memory, for instance, a disk drive. (See also virtual address.)

Protocol converter: a device that changes one computer or communications protocol into another.

Reduced-instruction-set computer (RISC): a computer in which the instruction set is simplified and minimized for rapid execution by specially designed hardware. (See also complex-instruction-set computer.)

Relational database: a method of storing information in which the relationship between different fields in a record is made explicit so that data can be updated and searched in terms of those relationships instead of record field locations.

Schematic capture: the entry or translation of a symbolic drawing of electronic circuitry into computer-readable digital format.

Shadow RAM: a special random-access-memory device that keeps a copy (shadow) of data taken from any memory location so that, if necessary, the data can be reinstated.

Small Computer Systems Interface (SCSI): an industry-standard high-speed interface for second-level storage systems.

SPECmarks: a normalized measure of performance for RISC systems based on a standard set of operations.

Specular reflection: light from one or more external sources reflected from solid objects. For computer-generated three-dimensional images, creating such reflections is a mathematically intense task.

Translation look-aside buffer: a buffer used with cache memory systems to hold recently completed translations of virtual to physical addresses. (See also physical address and virtual address.)

Virtual address: a binary address issued by a CPU that refers to the location of information in a primary level of memory, such as main memory. When data is copied from disk to main memory, the physical address (which see) is changed to the virtual address.

Wireframe: a means of illustrating a solid in which regularly spaced lines outline the volume of the solid, spaces between the lines are not filled in, and lines that would be hidden in a true solid are not removed.

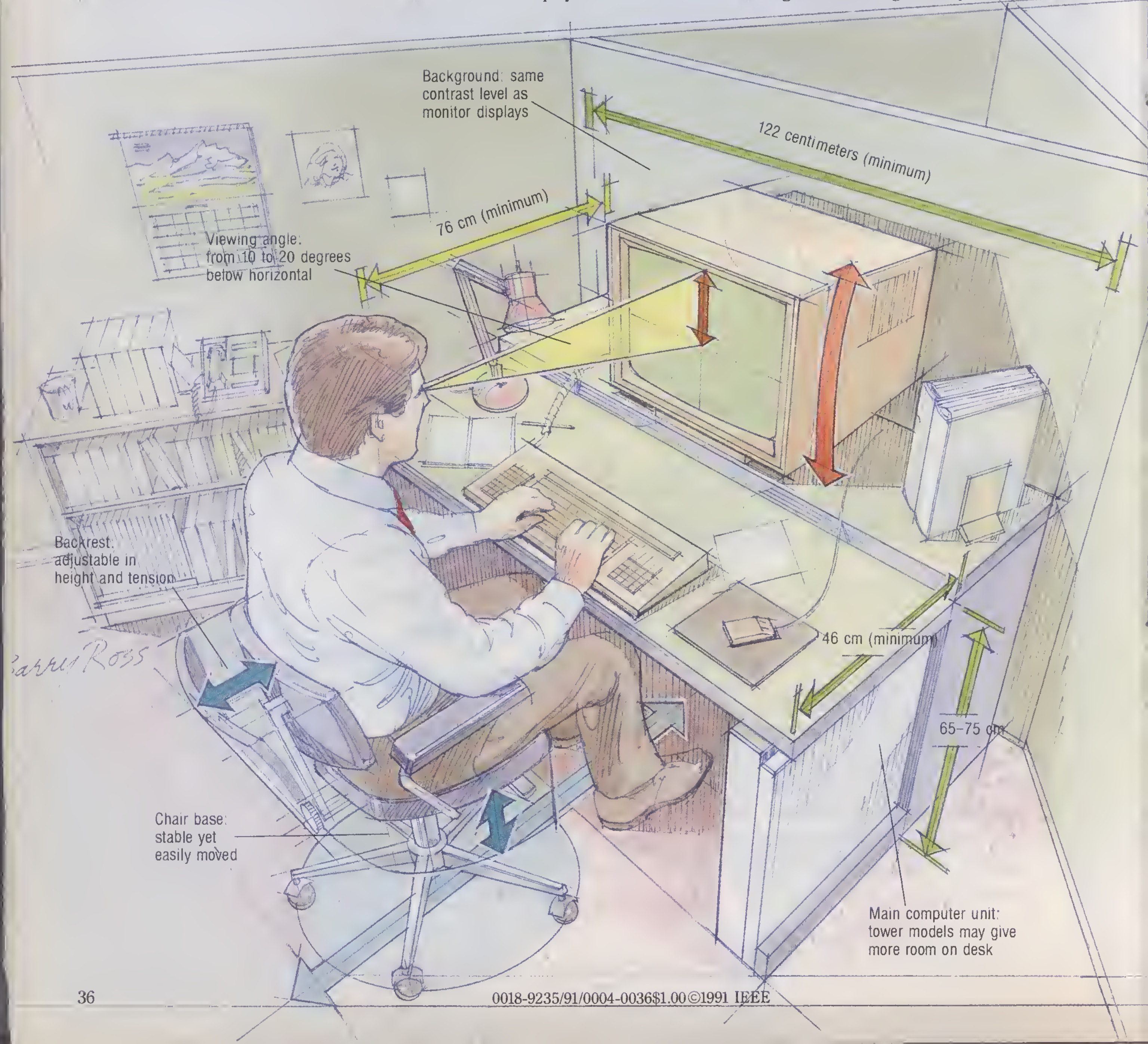
Tips on setting up your workstation

To promote efficiency and safety, the lighting must be right, desk and chair should be comfortable, and the layout convenient

Spectrum staff

In the wave of excitement about purchasing state-of-the-art workstations, it is easy to overlook the ergonomic aspects of the engineering environment. But engineers will have to live with workstations day in and day out, so it is important to take the physical layout of both the workspace and the workstation within it into account if a company wants to maximize the productivity and health of its employees.

While setting up the workstation to avoid eye and muscle fatigue may be the most important aspect of workplace design, what to do about reducing the effect of extremely low-frequency (ELF) magnetic fields is the most controversial. The IEEE's United States Activities Board states that, "At the present time [Aug. 13, 1990], there is no convincing evidence that VDT electric and magnetic fields significantly influence the



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health of VDT operators or adversely affect reproductive outcomes among pregnant women. However, further research is needed before a more conclusive statement can be made regarding the possible reproductive effects of factors associated with extensive use of VDTs.''

The chief focus of ELF concerns is the workstation monitor, whose under-100-hertz vertical deflection system can generate ELF fields. While magnetic field flux densities of below 1.0 microtesla, as are typical some 30 centimeters from a videodisplay terminal (VDT) screen, are deemed acceptable in Germany and England and by the International Radiation Protection Association, no standard for exposure levels has been established in the United States.

Unverified work done in Scandanavia has led some to suggest that ELF levels be below 0.2 μT. Recent studies of some commercial monitors found that field strength, which diminishes with distance, is generally below 0.2 μT at 76 cm (about arm's length) from the monitor's front and 122 cm from its sides and back. Responsible monitor manufacturers are beginning to specify ELF levels for their products. In the past, there have been vendors of display ''shields'' who led buyers to believe their product would reduce such emissions when it did not.

Since an office partition will not stop ELF emissions, workspaces should be set up so that no one in an adjoining area comes within 122 cm of the sides or back of a monitor in someone else's work area. (This meets the most stringent guidelines.) For adjoining groups of cubicles, centering a monitor at the back of a typical, 122-by-76-cm desktop and putting desks cattycorner in adjacent corners takes care of this.

FENDING OFF FATIGUE. Engineers will typically want a fairly large display because of the nature of the graphics material—schematic drawings and such—they work with. Some say that a 17-in. diagonal is the minimum acceptable, while others claim they need at least a 19-in. screen. The important thing is that information be easily readable.

The monitor should be situated so that, when the user is looking at it, his or her line of sight is between 10 and 20 degrees below the horizontal. This range seems to be most comfortable for users and helps prevents neck and back strain. Having the ability to tilt the monitor so that the display is perpendicular to the line of sight is a plus.

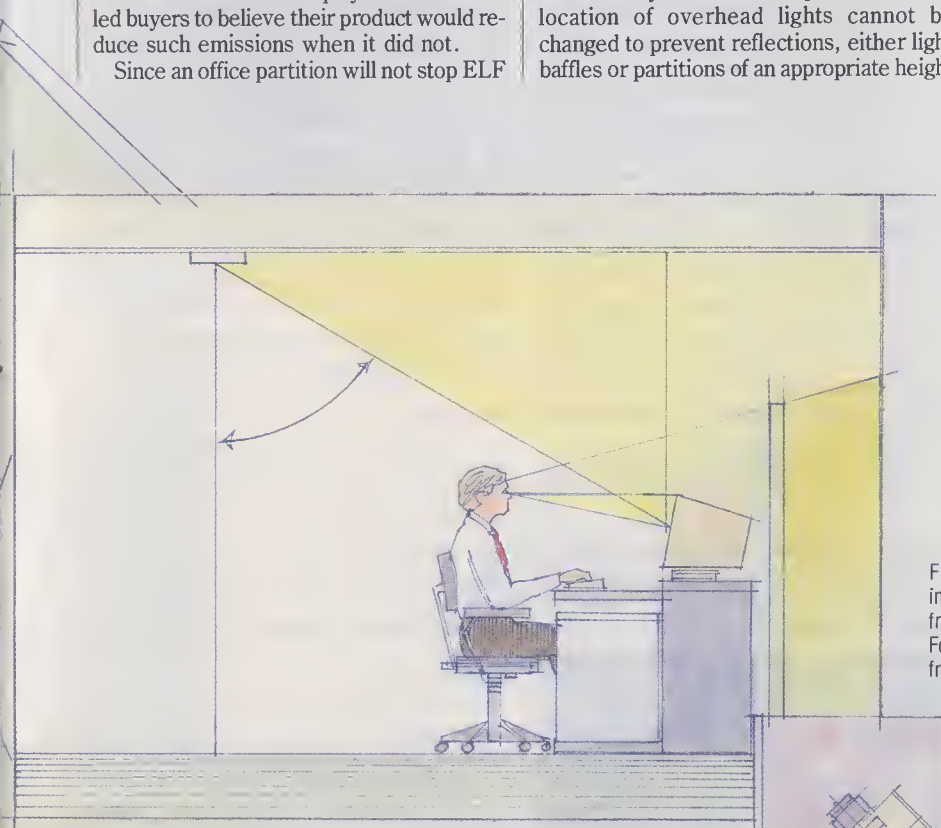
The monitor should also be positioned so that light from overhead fixtures or nearby windows is not reflected by the screen into the user's eyes. If that's not possible and the location of overhead lights cannot be changed to prevent reflections, either light baffles or partitions of an appropriate height should be installed. Similarly, window treatments should include adjustable blinds to prevent outside light reflections.

The area around the monitor that the user sees when his or her vision strays from the screen should be at the same luminance as the display to prevent eye strain (caused when the pupil must contract or dilate rapidly). Since most users will want to have a reasonably well-lit office, this implies that a predominantly light-colored display (that is, dark characters on a light background) is preferrable; it may also improve both visual acuity and depth of field. With a light screen, however, be sure that the scan rate is high enough to prevent flicker.

SITTING PRETTY. Office chairs should be adjustable to fit an individual's physical dimensions and provide good back support. A five-footed base is very stable, and casters will make it easier to move around.

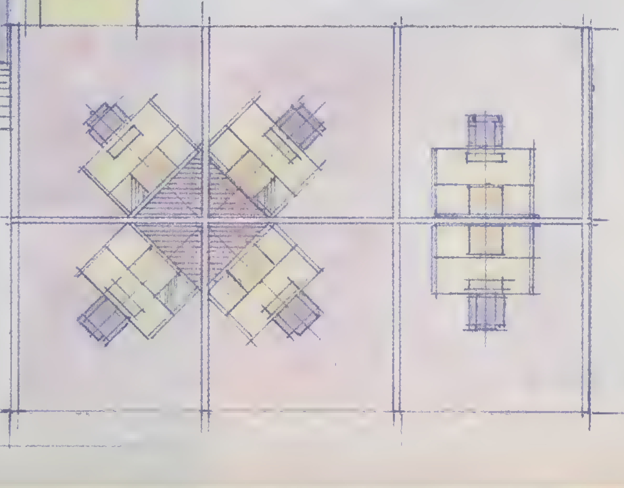
At minimum, a desk should allow leg room 64 cm high, 46 cm deep, and 51 cm wide. For most individuals a surface height between 65 and 75 cm is right for using a keyboard or mouse; if a desk is not adjustable in height, then 72 cm is a good compromise. A typical office desk is about 122 cm wide by 76 cm deep. However, if an engineer frequently uses large schematics, then the desk should be wider, perhaps as wide as 160 cm. There should also be room for a desk lamp so that reference materials can be lit well. Since there should be a minimum of 46 cm between the edge of the desk and the monitor, and since the monitor depth can exceed 30 cm, the desk may have to be deeper than 76 cm or the monitor put on a pedestal or shelf behind the desk.

No matter how comfortable the workspace is, a workstation user should remember to take a rest from screen work occasionally; taking five minutes to stretch the limbs and rest the eyes every couple of hours is a good practice. And since workstation use tends to be sedentary, getting in some exercise on the lunchbreak is a good idea. ◆



Lighting: angles of more than 60 degrees can cause glare. Use light baffles or partitions to correct lighting problems.

Floor plan: corner arrangement inherently prevents extremely low-frequency (ELF) emission problems. For facing arrangement, check distance from back of monitor to opposite user.



Source: the Department of Preventive Medicine of the University of Wisconsin, the National Research Council, and the National Lighting Bureau

Using workstations efficiently

Distributing computing power with workstations paves the way for concurrent engineering with high productivity

When computer specialists at Grumman Aerospace Corp.'s Aircraft Systems Division set out to devise a distributed computing environment tying together diverse design operations, they knew they were dealing with a hydra-headed monster. Over the years, various units within the division had computerized their operations, resulting in a vast array of computer-aided engineering tools and related software. But these systems were not necessarily designed to work together.

Moreover, mainframes and other centralized computing resources still played an essential role as a computing resource within the division—and they will continue to do so. But the move to localized computing power began long ago at Grumman, when workstations and personal computers first became available.

Now the task is to integrate these diverse resources into a fully distributed, data-driven environment, called the Grumman Computer/Information Integrated Enterprise (CIE). From a cost/performance perspective, one of the most important steps Grumman has already taken toward this goal is the introduction of the IBM RS6000 workstation. The introduction of these machines supporting computer-aided design (CAD) and computer-aided engineering (CAE) applications began last November in two Grumman facilities. Such leading two- and three-dimensional CAD/CAM software packages as Cadam and Catia, respectively, are already operating on these platforms, along with a large number of other applications.

To achieve the fully distributed environment, the computer specialists first assessed the available resources, determined the problems with the existing computing environment, and formulated a "workstation migration plan." As the name suggests, the decision was to maintain Grumman's CAD/CAM capabilities while controlling operating costs through effectively linked workstations. Crucial to the plan was the definition and implementation of a local-area network (LAN) strategy to link all the different types of machines together. Grumman's Data Systems Division played a key role in the integration of this environment. A major thrust was to cost-effectively optimize the computing tools available to the engineers, while promoting the systematic implementation of concurrent engineering among project teams.

Bernard I. Rachowitz, Richard K. Maue, Nicholas P. Angrisano, and Bill Abramson, Grumman Aerospace Corp.

An additional objective was to significantly reduce the number of hours in the current product development cycle while increasing product quality via an effective workstation environment. It is this strategy that will sustain the company as a competitive aerospace player and guarantee its role as a major supplier. As Grumman implements CIE, concerns in the product cycle are solved, further reducing costs and ensuring the company's competitive position.

NETWORK TASKS. The Grumman Aircraft Systems LAN had to integrate on a peer-to-peer basis an array of hardware with a mixture of different operating systems. It also had to ensure reliability by fulfilling the necessary data-transfer and up-time requirements. These requirements make automated file management a must. The systems included:

- A Cray supercomputer running under Unicos.
- Amdahl mainframes under MVS/XA and VM/XA.
- DEC minicomputers under VMS and Ultrix.
- Apollo workstations under Domain.
- IBM RS6000 workstations under AIX.
- Sun workstations under SunOS.
- IBM PCs and compatibles under MS-DOS.
- Macintosh personal computers under MacOS.

Members of the IBM RS6000 family, like the workstation shown here, figure prominently in Grumman's plans for its corporate technical environment.

IBM Corp.

The Cray, of course, plays the role of a high-end computational device for executing compute-intensive tasks in such areas as fluid dynamics and structural mechanics, while the Amdahl mainframes serve mainly as the engine for systems that support the division's business function. The DEC computers are employed in various laboratories, as well as front-ending some of the large mainframes conducting special-purpose investigative projects and data analysis.

The Apollo workstations are used mainly for software development projects and as platforms for running Mentor Graphics circuit-design and -analysis software.

Currently the IBM RS6000 workstations are primarily used to run Cadam and Catia geometric design codes, as well as for analysis and for numerical-control manufacturing work. But their use is spreading into other areas—in fact, Grumman was the first to use RS6000s for production CAD/CAM applications.

The personal computers, both IBM and Macintosh types, are used for word processing, spreadsheet analysis, and office communications tasks.

This migration of certain functions from large centralized mainframes and minicomputers to a distributed LAN-based computing environment supports the Grumman concept of employees working in "task teaming groups," the company's term for concurrent engineering. The resulting synergy from co-locating members of various disciplines (aerodynamics, structural design and analysis, manufacturing, test engineering, and business functions) has greatly reduced the overall calendar time from design concept to product fabrication.

Today's LAN is an Ethernet-based network. The Transmission Control Protocol/Internet Program (TCP/IP) was chosen because it provided a ubiquitous basis for establishing connectivity between the many Grumman systems. TCP/IP also puts Grumman in an advantageous position for migrating to the Open Systems Interconnec-

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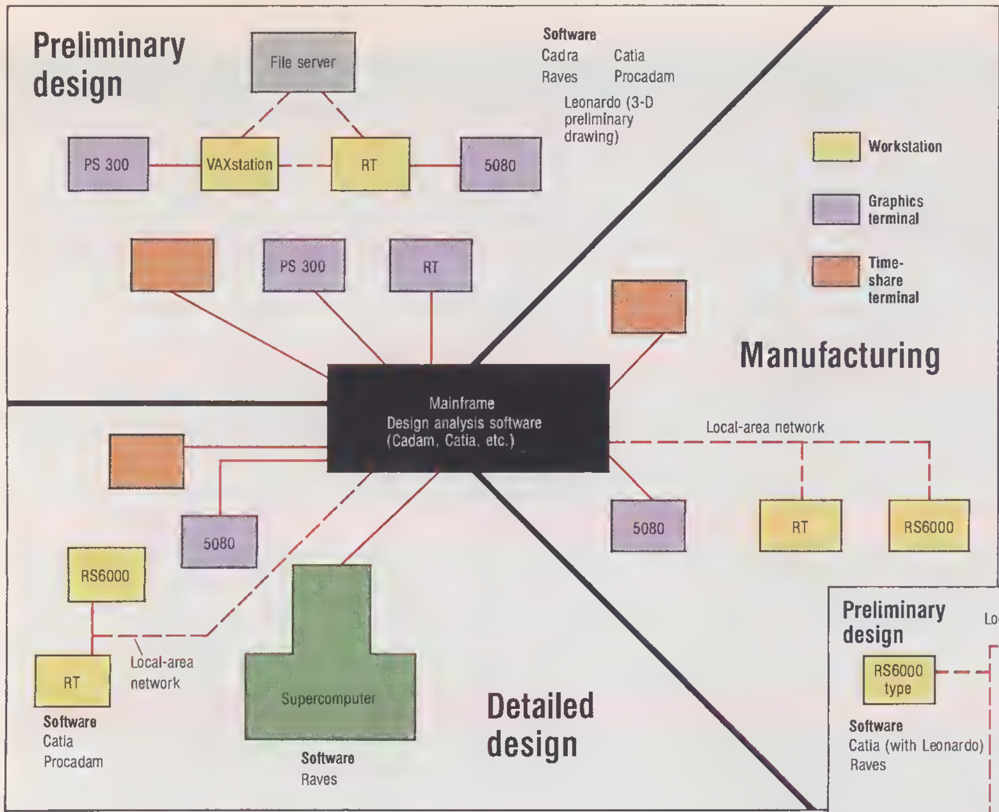

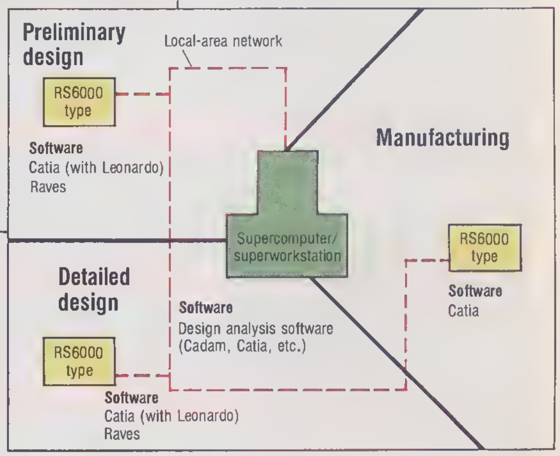

How Grumman's system will grow

The present Grumman environment (left) is a mixture of workstations, graphics terminals, and time-share terminals connected by direct links as well as local-area networks (LANs); both a mainframe and a supercomputer provide support for compute-intensive tasks. In the future (below), engineers will rely more heavily on distributed computing in the form of workstations and supercomputers linked solely by LANs.

tion (OSI) protocols in the near future.

Ethernet is supported on most of the computing platforms at Grumman. Virtually all of the Department of Defense and other U.S government agencies and universities that Grumman interfaces with have Ethernet TCP/IP LANs. The TCP/IP protocol is also supported by many vendors.

At Grumman, the Ethernet LAN is extended between sites or buildings by means of fiber optics or microwave or leased telephone lines for off-campus links.

Grumman has native TCP/IP protocol on all of its LAN computers, including Amdahl mainframes running MVS/XA and VM/XA with extensions to the Telnet software application providing IBM Systems Network Architecture (SNA) 3270 terminal emulation. A key aid is a Mitek Corp. TCP/IP-to-SNA protocol converter handling special applications that do not yet have TCP/IP support.

TODAY'S SETUP. At Grumman, much of the current environment has evolved over time and is the product of numerous factors contributing to a technically strong collection of sophisticated design automation tools. Elements such as autonomy for different aircraft-development projects led to the use of a myriad of tools for electronic CAD (ECAD) and CAM. Within the corporate toolbox may be found items from Cadam, Calay, Calma, Computervision, Daisy, Futurenet, Mentor Graphics, P-CAD, and Prance for use in the electronic design process. Of major significance is the fact that only a few of these tools are integrated with others, so that most are not able to share data interactively. Were there a universally supported CAE framework for commercial tools, it would be simple to add new tools to the system and have them work with those already present.

In conjunction with these purchased tools, many in-house systems have been developed because commercially available packages for some specific requirements were either nonexistent or inadequate. Systems for drawings release and control, parts lists, methods, and logistic support are several examples. At some time during the production cycle, all of these systems are required to interface with the purchased tools for ECAD.

In all instances, the procured ECAD systems matched quite well with their intended purpose. Schematic capture, digital design, behavioral modeling, digital fault simulation, and automatic test generation were just some of the capabilities used to design ICs, hybrids, printed wiring boards (PWBs), flex circuits, wirewrap assemblies, avionics boxes, and test stations.

In retrospect, the CAE procurements of the late 1970s and early 1980s were primarily user driven and automated only what was particularly problematic at that time. These selective CAE decisions demonstrated an effective return on investment and great improvements in product quality. Two examples: a PWB system reduced bare-board rejection rates from 38 percent to under 1 percent; circuit design tasks were reduced by 25 percent by utilizing schematic capture and digital simulators, among other tools.

Today, the return on investment could easily be extended by addressing the product requirements of all disciplines in the CAE process (for example, engineering's packaging needs, manufacturing's need to interface with automatic insertion tools and various test equipment, and technical publications' task of generating maintenance manuals). Factors that then constrained the total return on investment were the actual tools, which by their technical nature limited the electronic CAD integration that the users required.

As the decade progressed, both hardware and software vendors became more sensitive to the demands for tool integration as specified by the customer. Elimination of proprietary hardware and operating systems, inconsistent data formats, unique databases and libraries, and the lack of consistent support for standards were among those concerns. The technology development and division computing department recognized that the emerging technologies would support the required CAE system—one that had the ability to transfer and reuse valuable data.

PAST PROBLEMS. Before embarking on the strategy for the shared-data distributed en-

(Continued on p. 48)

Representative sample of commercially available workstations

Performance ratings	Central processing unit	Operating systems[1]	Floating-point accelerator	Memory[2]	Hard drive[1,3]	Tape backup[4]	Compact-disc ROM	Graphics adapter[1]	Monitor[1,5]	Interfaces[1,6]	Other features and options
Acer America Corp., 1170, $4495, 3 days ARO											
11+ MIPS	CISC, Intel 80486	MS-DOS 3.3 (Unix)	On CPU chip	R: 4–64M, 85 ns	200M, IDE	N.A.	N.A.	VGA	C: 14 in., 1024 × 768	(E), RS2, I48	
American Mitac Corp., 4280G, $7995, 2 days											
14.7 MIPS	CISC, Intel 80486	MS-DOS 4.01	(Weitek 4167 on CPU board)	C: 8–256K, 25 ns R: 4–64M, 80 ns	(330–660M, SCSI)	N.A.	N.A.	Super VGA	(C: 14 in., 1024 × 768)	(E), (TR), RS2, (RS4), (I48), (C)	Novell-, Banyan-, and Unix-compatible file server
Apple Computer Inc., Macintosh IIfx, M5515LL/A, $8969–$10 969, immediate											
N.A.	CISC, Motorola 68030	MacOS 6.0.7 (A/UX)	Motorola 68882 on CPU board	C: 32K, 25 ns R: 4–8M, 80 ns	80M, SCSI (160M, SCSI)	S	O	NuBus	C: 13 in., 640 × 480 (M: 15 in., 640 × 870)	(E), (TR), RS2, RS4, (I48), (C)	Can take OOS, OS/2 files, SCSI/OMA controller; 2 I/O processors
Arche Technologies Inc., Arche Legacy 486-33, $6755–$7995, immediate											
21.5 MIPS, 1.56 MFLOPS, 37 790 AIM Ohrystones	CISC, Intel 80486	MS-OOS 3.3 (MS-OOS 4.01), SCO Unix, Interactive Unix, OS/2, V1.2	Weitek 4167 on CPU chip	C: 256K, 20 ns R: 4–64M, 80 ns	(338M, ESOI)	O	O	(VGA)	(14 in., 640 × 480 or 800 × 600)	(E), (TR), (RS2), (RS4), (I48), C	Transparent direct-memory-access snooping, intelligent cache controller, 4-level write posting, burst mode
AT&T Computer Systems, Starserver, $14 995–$21 495, 21 days											
26.5 MIPS	CISC, Intel 80486	Unix (MS-OOS, OS/2, Simultask)	Intel 80387 on CPU board	C: 8K or 128K, 20 ns R: 8–64M, 20 ns	300M, SCSI (1G, SCSI)	S	S	Super VGA	17 in., 1280 × 1024 (20 in., 1024 × 768)	(E), (TR), RS2, RS4	Up to 36G-byte hard-disk storage
Commodore Business Machines Inc., Amiga 3000UX, $5499–$6999											
5 MIPS	CISC, Motorola 68030	Unix V.4	Motorola 68882 on CPU board	R: 4–16M, 30 ns	105M, SCSI (210M, SCSI)	O	N.A.	N.A.	(C: 14 in., 800 × 600)	E, RS2, C	
Compaq Computer Corp., DeskPro 486/33L, $10 999, immediate											
11.2 SPECmarks, 16 234 khornerstones	CISC, Intel 80486	(OOS, OS/2, Unix)	On CPU chip	C: 8K on chip plus 128K, 25 ns R: 4–100M, 80 ns	120 and 210M, IDE 320 and 650M, ESOI	O	N.A.	VGA (Advanced Graphics System)	(C: 16 in., 1024 × 768) (M: 14 in., 640 × 480)	(TR), RS2, C	Maximum drive storage 2.6G, can use fixed-disk drive arrays
CompuAdd Corp., CompuAdd SS1, $5995–$11 995											
12.5 MIPS, 1.4 MFLOPS	RISC, LSI Logic Sparkit 20	SunOS 4.1	Weitek 3170A on CPU board	C: 64K, 25 ns R: 8–64M, 100 ns	(200M, SCSI)	O	N.A.	Custom	M: 19 in., 1152 × 900 (C: 16/19 in., 1152 × 900)	E, RS2	3 internal 3-1/2-in. SCSI drive bays
Concurrent Computer Corp., Series 7000, $23 000–$80 000, 45 days ARO											
20–60 MIPS, 2.5–7.5 MFLOPS	CISC, Motorola 68040	Real-time Unix	On CPU chip	C: 8K, on chip R: 8–128M, 4 ns	200M–2146M, SCSI (850M, IPI2)	O	N.A.	VGA	M: 16 in., 1024 × 768 (C: 19 in., 1280 × 1024)	E, (TR), RS2, (RS4), (I48), (C)	For real-time operation, 480-/640-ns-resolution clock
Control Data Corp., 910B-48X, $21 500–$31 500, 6 weeks											
33 MIPS, 6.0 MFLOPS, 23 SPECmarks	RISC, MIPS R3000A	Custom, Irix 3.3.2	MIPS R3010A on CPU board	C: 128K, 20 ns R: 8–128M, 20 ns	200M, SCSI (1.2G, SCSI)	O	N.A.	Custom	C: 14 in., 1024 × 768 (C: 19 in., 1280 × 1024)	E, RS2, (I48), C, (FOOI)	Options: dial and buttons box, digitizer tablet, Genlock, NTSC or PAL
Copam USA Inc., 486-25, $5399–$12 500, 7 days											
11 MIPS	CISC, Intel 80486	MS-OOS 4.01	On CPU board	C: 64–256K, 25 ns R: 2–32M, 80 ns	155M, ESOI, SCSI (335M, ESOI, SCSI)	N.A.	N.A.	(Varies)	C: 14 in., 1024 × 768	E, RS2, C	EISA controller standard

1 Terms in parentheses indicate options offered by vendors. 2 C = cache, R = RAM; capacity in bytes; access time.
3 Capacity in bytes; IDE = Interactive Data Entry, SCSI = Small Computer Systems Interface, ESDI = Enhanced Small Disk Interface, IPI = Intelligent Peripheral Interface.
4 O = optional, S = standard, N.A. = not available from the vendor. 5 C = color, M = monochrome, resolution in pixels.
6 E = Ethernet, TR = token ring, RS2 = RS-232C, RS4 = RS-422, I48 = IEEE-488, C = Centronics/parallel, FDDI = Fiber Distributed Data Interface.

Representative sample of commercially available workstations (continued)

Performance ratings	Central processing unit	Operating systems	Floating-point accelerator	Memory[2]	Hard drive[1, 3]	Tape backup[4]	Compact-disc ROM	Graphics adapter[1]	Monitor[1, 5]	Interfaces[1, 6]	Other features and options
Dell Computer Corp., System 433TE, $8549–$20 495, 3–5 weeks											
14.5 MIPS, 10.8 SPECmarks	CISC, Intel 80486	(MS-DOS, OS/2, Unix)	On CPU chip (Weitek 4167-33 on CPU board)	C: 128K, 20 ns R: 4–64M, 80 ns	80M, IDE (650M, ESDI)	O	N.A.	VGA	M: 12 in., 640 × 480 (C: 19 in., 1280 × 1024)	(E), RS2, C	Drive array optional, 350-/525M-byte internal or external tape backups
										E, RS2, (RS4), (C), (FDDI), (VME)	Optional digitizer tablet, dial box, button box
										RS2, C	Portable workstation, gas plasma monitor, options include: 640-by-480-pixel thin-film transistor color display, 200M-byte hard-disk drive, tape back-up unit, built-in 2400-baud modem
										E, RS2	A parallel-processing system that can have 4–16 T800 transputer or i860 nodes, CPU board includes i860 coprocessor
										E, RS2, VME, (FDDI)	3-D graphics standard, upgradable, optional digitizer tablet and control dials
14.38 MIPS	CISC, Intel 80486	MS-DOS 4.01 (NetWare 3.1, Unix, Xenix, OS/2)	On CPU chip	C: 64–512K, 15 ns R: 4–96M, 70 ns	338M, ESDI (338M, SCSI)	S&O	O	Super VGA	14 in., 1024 × 768 (16 in., 1024 × 768)	(E), (TR), RS2, (RS4), (I48), C	Optional: graphics tablet, WORM drive, OSP cards, I/O cards
Hewlett-Packard Co., HP/Apollo 9000 Model 425T, $8890–$33 390, 8 weeks											
20 MIPS, 2.6 MFLOPS, 11 SPECmarks	CISC, Motorola 68040	HP-UX 7.05, Domain/OS	On CPU chip	C: 8K, 40 ns R: 8–64M, 80 ns	400M, SCSI	S	S&O	VRX	C: 16 in., 1280 × 1024 (C: 19 in., 1280 × 1024)	E, (TR), RS2, I48, C	
Intergraph Corp., Series 2000, $15 900–$36 300, 120 days ARO											
12.5 MIPS, 1.03 DP MFLOPS	RISC, Intergraph C300	Unix 3.1 (MS-DOS 3.3)	Intergraph on CPU board	C: 8K, 38–57 ns R: 4–64M, 100 ns	200M, SCSI (800M, SCSI)	O	O	Custom	C: 19 in., 1184 × 884 (dual 19-in. configuration)	E, RS2, (C)	Supports external peripherals, available as console, desktop, or digitizing model
International Business Machines Corp., Power Station 530, $45 000–$150 000+, 30 days											
37.1 MIPS, 13.7 MFLOPS, 32.0 SPECmarks	RISC, custom	Custom, AIX 3.1	On CPU chip	C: 64K R: 16–512M	355M, SCSI (857M, SCSI)	O	O	Custom	(M: 19 in., 1280 × 1024; C: 23 in., 1280 × 1024)	(E), (TR), RS2, (RS4), (I48), C	
Laser Digital Inc., Pacer Super Workstation 486/33, $4800–$5000, 5–7 days											
14 MIPS	CISC, Intel 80486	OS/2, MS-DOS 3.30, Unix, PC-MOS, (Xenix)	Weitek 4167 on CPU board	C: 128–256K, 20 ns R: 16–64M, 70 ns	143M, SCSI	O	O	VGA	C: 14 in., 1024 × 768	E, (TR), RS2, (RS4), (I48), C	Options: larger hard drives, WORM drive, modems

Representative sample of commercially available workstations

Performance ratings	Central processing unit	Operating systems[1]	Floating-point accelerator	Memory[2]	Hard drive[1, 3]	Tape backup[4]	Compact-disc ROM	Graphics adapter[1]	Monitor[1, 5]	Interfaces[1, 6]	Other features and options
Acer America Corp., 1170, $4495, 3 days ARO											
11+ MIPS	CISC, Intel 80486	MS-DOS 3.3 (Unix)	On CPU chip	R: 4–64M, 85 ns	200M, IDE	N.A.	N.A.	VGA	C: 14 in., 1024 × 768	(E), RS2, I48	
American Mitac Corp., 4280G, $7995, 2 days											
14.7 MIPS	CISC, Intel 80486	MS-DOS 4.01	(Weitek		(330-	N.A.	N.A.	Super VGA	(C: 14 in.,		
Apple Computer Inc., Macintosh IIfx,											
N.A.	CISC, Motorola 68030	MacOS 6.0.7 (A/UX)									
Arche Technologies Inc., Arche Legacy											
21.5 MIPS, 1.56 MFLOPS, 37 790 AIM Dhrystones	CISC, Intel 80486	MS-DOS 3.3 (MS-DOS 4.01), SCO Unix, Interactive Unix, OS/2, V1.2									
AT&T Computer Systems, Starserver,											
26.5 MIPS	CISC, Intel 80486	Unix (MS-DOS, OS/2, Simultask)									
Commodore Business Machines Inc.,											
5 MIPS	CISC, Motorola 68030	Unix V.4									
Compaq Computer Corp., DeskPro 486											
11.2 SPECmarks, 16 234 khornerstones	CISC, Intel 80486	(DOS, OS/2, Unix)		100M, 80 ns					480)		
CompuAdd Corp., CompuAdd SS1, $5995–$11 995											
12.5 MIPS, 1.4 MFLOPS	RISC, LSI Logic Sparkit 20	SunOS 4.1	Weitek 3170A on CPU board	C: 64K, 25 ns R: 8–64M, 100 ns	(200M, SCSI)	0	N.A.	Custom	M: 19 in., 1152 × 900 (C: 16/19 in., 1152 × 900)	E, RS2	3 internal 3-1/2-in. SCSI drive bays
Concurrent Computer Corp., Series 7000, $23 000–$80 000, 45 days ARO											
20–60 MIPS, 2.5–7.5 MFLOPS	CISC, Motorola 68040	Real-time Unix	On CPU chip	C: 8K, on chip R: 8–128M, 4 ns	200M–2146M, SCSI (850M, IPI2)	0	N.A.	VGA	M: 16 in., 1024 × 768 (C: 19 in., 1280 × 1024)	E, (TR), RS2, (RS4), (I48), (C)	For real-time operation, 480-/640-ns-resolution clock
Control Data Corp., 910B-48X, $21 500–$31 500, 6 weeks											
33 MIPS, 6.0 MFLOPS, 23 SPECmarks	RISC, MIPS R3000A	Custom, Irix 3.3.2	MIPS R3010A on CPU board	C: 128K, 20 ns R: 8–128M, 20 ns	200M, SCSI (1.2G, SCSI)	0	N.A.	Custom	C: 14 in., 1024 × 768 (C: 19 in., 1280 × 1024)	E, RS2, (I48), C, (FDDI)	Options: dial and buttons box, digitizer tablet, Genlock, NTSC or PAL
Copam USA Inc., 486-25, $5399–$12 500, 7 days											
11 MIPS	CISC, Intel 80486	MS-DOS 4.01	On CPU board	C: 64–256K, 25 ns R: 2–32M, 80 ns	155M, ESDI, SCSI (335M, ESDI, SCSI)	N.A.	N.A.	(Varies)	C: 14 in., 1024 × 768	E, RS2, C	EISA controller standard

1 Terms in parentheses indicate options offered by vendors. 2 C = cache, R = RAM; capacity in bytes; access time.
3 Capacity in bytes; IDE = Interactive Data Entry, SCSI = Small Computer Systems Interface, ESDI = Enhanced Small Disk Interface, IPI = Intelligent Peripheral Interface.
4 D = optional, S = standard, N.A. = not available from the vendor. 5 C = color, M = monochrome, resolution in pixels.
6 E = Ethernet, TR = token ring, RS2 = RS-232C, RS4 = RS-422, I48 = IEEE-488, C = Centronics/parallel, FDDI = Fiber Distributed Data Interface.

Representative sample of commercially available workstations (continued)

Performance ratings	Central processing unit	Operating systems	Floating-point accelerator	Memory[2]	Hard drive[1, 3]	Tape backup[4]	Compact-disc ROM	Graphics adapter[1]	Monitor[1, 5]	Interfaces[1, 6]	Other features and options
Dell Computer Corp., System 433TE, $8549–$20 495, 3–5 weeks											
14.5 MIPS, 10.8 SPEC-marks	CISC, Intel 80486	(MS-DOS, OS/2, Unix)	On CPU chip (Wei-tek 4167-33 on CPU board)	C: 128K, 20 ns R: 4–64M, 80 ns	80M, IDE (650M, ESDI)	0	N.A.	VGA	M: 12 in., 640 × 480 (C: 19 in., 1280 × 1024)	(E), RS2, C	Drive array optional, 350-/525M-byte internal or external tape backups
Digital Equipment Corp., DECstation Model 200CX, $14 995, immediate											
24 MIPS, 6.4 single-precision (SP)/3.7 DP MFLOPS, 18.5 SPEC-marks	RISC, MIPS R3000	Ultrix-32, V4.1	MIPS R3010 on CPU board	C: 128K, 15 ns R: 8–120M	(665M-21G, SCSI)	S	Custom		M: 19 in., 1024 × 864 (M/C: 16/19 in., 1280 × 1024)	E, RS2, (RS4), (C), (FOOI), (VME)	Optional digitizer tablet, dial box, button box
Dolch Computer Systems, PAC 486-33E, $14 995, 10 working days											
14.5 MIPS	CISC, Intel 80486	OOS 4.0.1 (Unix)	Weitek 4167 on CPU board	R: 2–32M, 70 ns	100M, SCSI (200M, SCSI)	N.A.	N.A.	VGA (Super VGA)	M: 9 in., 640 × 400 (C: 11¼ in., 640 × 480)	RS2, C	Portable workstation, gas plasma monitor, options include: 640-by-480-pixel thin-film transistor color display, 200M-byte hard-disk drive, tape back-up unit, built-in 2400-baud modem
EE International Computer Corp., EEC-1, $18 000–$40 000, 45 days											
160 MIPS, 320 MFLOPS	RISC, Intel 80486 and i860, Inmos T800	Unix V-4 (MS-DOS)	Dn CPU chip	C: 128K R: 8–16M, 80 ns	150M, ESDI (600M, SCSI)	0	N.A.	VGA	C: 14 in., 1024 × 768	E, RS2	A parallel-processing system that can have 4–16 T800 transputer or i860 nodes, CPU board includes i860 coprocessor
Evans & Sutherland Design Systems Division, ESV 3/32, $27 900–$95 000, 30 days											
24 MIPS, 4.0 MFLDPS, 17.3 SPEC-marks	RISC, MIPS R3000	Custom, ES/OS 2.0	MIPS R3010 on CPU board	C: 128K R: 8–128M	(1200M, SCSI)	D	N.A.	Custom	C: 19 in., 1280 × 1024	E, RS2, VME, (FDDI)	3-D graphics standard, upgradable, optional digitizer tablet and control dials
Fortron/Source Corp., Net Set 486/33E, $6150, 5 days											
14.38 MIPS	CISC, Intel 80486	MS-DDS 4.01 (NetWare 3.1, Unix, Xenix, OS/2)	On CPU chip	C: 64–512K, 15 ns R: 4–96M, 70 ns	338M, ESDI (338M, SCSI)	S&D	D	Super VGA	14 in., 1024 × 768 (16 in., 1024 × 768)	(E), (TR), RS2, (RS4), (I48), C	Optional: graphics tablet, WORM drive, DSP cards, I/D cards
Hewlett-Packard Co., HP/Apollo 9000 Model 425T, $8890–$33 390, 8 weeks											
20 MIPS, 2.6 MFLOPS, 11 SPEC-marks	CISC, Motorola 68040	HP-UX 7.05, Oomain/OS	On CPU chip	C: 8K, 40 ns R: 8–64M, 80 ns	400M, SCSI	S	S&O	VRX	C: 16 in., 1280 × 1024 (C: 19 in., 1280 × 1024)	E, (TR), RS2, I48, C	
Intergraph Corp., Series 2000, $15 900–$36 300, 120 days ARO											
12.5 MIPS, 1.03 DP MFLOPS	RISC, Intergraph C300	Unix 3.1 (MS-DOS 3.3)	Intergraph on CPU board	C: 8K, 38–57 ns R: 4–64M, 100 ns	200M, SCSI (800M, SCSI)	0	0	Custom	C: 19 in., 1184 × 884 (dual 19-in. configuration)	E, RS2, (C)	Supports external peripherals, available as console, desktop, or digitizing model
International Business Machines Corp., Power Station 530, $45 000–$150 000+, 30 days											
37.1 MIPS, 13.7 MFLDPS, 32.0 SPEC-marks	RISC, custom	Custom, AIX 3.1	Dn CPU chip	C. 64K R: 16–512M	355M, SCSI (857M, SCSI)	0	0	Custom	(M: 19 in., 1280 × 1024; C: 23 in., 1280 × 1024)	(E), (TR), RS2, (RS4), (I48), C	
Laser Digital Inc., Pacer Super Workstation 486/33, $4800–$5000, 5–7 days											
14 MIPS	CISC, Intel 80486	OS/2, MS-DDS 3.30, Unix, PC-MOS, (Xenix)	Weitek 4167 on CPU board	C:128–256K, 20 ns R:16–64M, 70 ns	143M, SCSI	0	D	VGA	C: 14 in., 1024 × 768	E, (TR), RS2, (RS4), (I48), C	Options: larger hard drives, WORM drive, modems

Representative sample of commercially available workstations (continued)

Performance ratings	Central processing unit	Operating systems[1]	Floating-point accelerator	Memory[2]	Hard drive[1, 3]	Tape backup[4]	Compact-disc ROM	Graphics adapter[1]	Monitor[1, 5]	Interfaces[1, 6]	Other features and options
Mars Microsystems Inc., Mariner 4i, $6295–$11 995, 30–60 days											
17.3 MIPS, 12.3 SPECmarks	CISC, Cypress CY7C601/ Intel 80386	SparcOS 4.x (MS-00S 3.3/4.1)	Cypress CY7C602 /Intel 80387 on CPU board	C: 64K, 25 ns R: 2–96M, 100 ns	209M, SCSI	D	D	VGA	19 in., 1152 × 900 (19 in., 1152 × 900)	E, (TR), RS2, (RS4), (I48), (C)	
Microway Inc., Number Smasher-486/T, $5800, 3–5 days											
14.5 MIPS, 2.1 0P MFLOPS, 16 Megawhetstones	CISC, Intel 80486	MS-DDS (Unix)	(Weitek 4167 on CPU board)	C: 8K, internal R: 4–16M, 60–100 ns	150M, SCSI (330M–1.2G, I0E)	N.A.	N.A.	VGA	N.A.	RS2, C	Comes in ISA or EISA versions, 256-K external cache and 64M maximum RAM on EISA version
Micro Express, ME 486-ISA/33, $4500–$9500, 1 week											
N.A.	CISC, Intel 80486	MS-DDS 4.01	Dn CPU chip	C: 256K, 25 ns R: 4–64M, 80 ns	200M, IDE (750M, ESOI)	D	0	Extended VGA	C: 14 in., 1024 × 768	(E), (TR), RS2, (RS4), (I48), C	
MIPS Computer Systems Inc., Magnum 3000, $8990–$50 000, 30 days											
30.8 MIPS, 18.6 SPECmarks	RISC, MIPS R3000	Custom, RISC/os	MIPS R3010 on CPU board	C: 64–64K, 20 ns R: 8–128M, 70–100 ns	(6G, SCSI)	S	N.A.	Custom	M: 17 in., 1152 × 900; C: 16/19 in., 1280 × 1024	E, (TR), RS2, (C)	Board is upgradable to next-generation technology
Mobius Computer Corp., Protege Series PWS/433, $11 093–$16 000, 7–10 days											
18 MIPS, 1.5 MFLOPS, 12 SPECmarks	CISC, Intel 80486	AT&T Unix System V3.2	Weitek 4167-33 on CPU board	C: 8K, internal R: 4–16M, 70 ns	105M, SCSI (210–600M, SCSI)	0	0	Advanced Graphics System	(C: 16 in., 1024 × 768) (C: 17 in., 1280 × 1024)	E, RS2, C	2-D graphics accelerator is standard feature
NCR Corp., System 3000, Model 3345, $13 795–$49 485, 1 week											
27 MIPS, 1.63 SP/1.33 0P MFLOPS	CISC, Intel 80486	(MS-D0S 4.0, OS/2, Unix)	On CPU chip (Weitek 4167 on CPU board)	R: 4–64M, 80 ns	(100–340M, SCSI)	N.A.	S&D	VGA	(M: 14 in., 640 × 480; C: 16 in., 1024 × 768)	(E), RS2, C	
Polywell Computers Inc., Poly 486-33EISA, $6500–$18 000, 10 days											
14.4 MIPS	CISC, Intel 80486	MS-00S 3.3 or 4.01 (OS/2, Unix, NetWare 3.1)	Weitek 4167 on CPU board	C: 256K, 15 ns R: 4–16M, 70 ns	207M, IDE (200–667M, ESDI) (1–2.5G, SCSI)	S	D	VGA	C: 14 in., 1024 × 768	(E), (TR), RS2, (RS4), C	EISA Ethernet, EISA TIGA graphics card
Ramtek Corp., Millennium, N.A., 90 days ARO											
30 MIPS, 80 MFLOPS	RISC, Sparc Engine	SunOS	Custom, on separate board	C: 16K, 40 ns R: 40M–1.4G, 80 ns	773M, SCSI	N.A.	N.A.	Custom	C: 19 in., 1280 × 1024	E, RS2	Frame grabber for RS170 video
RDI Inc., Brite Lite Laptop, $10 800, 30 days											
15.8 MIPS, 1.6 MFLOPS, 10.0 SPECmarks	RISC, Sun Sparc	SunOS 4.1.1 (Mac OS 6.0.6)	Weitek on CPU board	C: 64K, 80 ns R: 8–48M, 60 ns	120M, SCSI (200M, SCSI)	N.A.	N.A.	Custom	M LCD: 10.5 in., 1152 × 900; C LCD: 12.8 in., 1024 × 768	E, RS2, (RS4)	Battery-powered
Silicon Graphics Inc., 4D135, $21 000–$31 000, 30 days or less											
35 MIPS, 6 MFLOPS, 23 SPECmarks	RISC, MIPS R3000A	Custom, Irix 3.3	MIPS R-3010A on CPU board	C: 128K R: 8–128M	(200M–1.2G, SCSI)	D	N.A.	Custom	C: 19 in., 1280 × 1024 (C: 14 in., 1024 × 768)	E, RS2, (I48), C	Dptions include dials and buttons box and digitizer tablet
Solarix Systems, Solarix/4 Personal Workstation Plus, $6996–$12 290, 4 weeks											
18 MIPS, 3 MFLOPS, 12 SPECmarks	RISC, Cypress 4.03 CY7C601	SolarixOS	Cypress CY7C602 on CPU board	C: 64–256K, 25 ns R: 8–128M, 80 ns	104M, SCSI	S	S	Custom	C: 19 in., 1152 × 900 (C: 16 in., 1152 × 900)	E, RS2, C	

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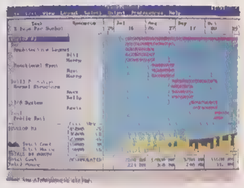

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Representative sample of commercially available workstations (continued)

Performance ratings	Central processing unit	Operating systems[1]	Floating-point accelerator	Memory[2]	Hard drive[1,3]	Tape backup[4]	Compact-disc ROM	Graphics adapter[1]	Monitor[1,5]	Interfaces[1,6]	Other features and options
Solbourne Computer Inc., S4000 Desktop Workstation, $8995-$30 000, 30 days											
25.5 MIPS, 1.7 MFLOPS, 13.1 SPEC marks	RISC Panasonic MN10501	OS/MP, custom version of SunOS	On CPU chip	C: 8K R: 8–104M, 60 ns	(Dual 200M, SCSI)	0	N.A	Custom	M: 19 in., 1152 × 900 (C: 16 or 19 in., 1152 × 900)	E, RS2	
Sony Microsystems Co., NEWS 3250 Workstation, $9900-$11 900, 2 weeks											
17 MIPS, 1.8 MFLOPS, 11.3 SPEC-marks	RISC, MIPS R3000	NEWS-OS 5.0	MIPS R3010 on CPU board	C: 64K R: 4–36M, 8 ns	240M, SCSI (406M, SCSI)	0	0	Custom	M LCD: 11 in., 1120 × 780	E, RS2, C	Optional magneto-optical drive, digital audio tape, CD writer
Star Technologies Inc., Star 910/VP Compute Server, $99 990-$265 450, 90 days											
40 MIPS, 160-SP/80-DP MFLOPS	RISC, Cypress CY7C601	StarOS 4.0.3 (SunOS 4.0)	Cypress CY7C602 on CPU board	C: 1M R: 32–256M	776M, SCSI (1.15G, IPI)	N.A.	N.A.	N.A.	N.A.	E, RS2	Optional vector processor board
Stardent Computer Inc., Stardent 3000VS Visualization System, $109 000-$239 000, 60 days											
128 MIPS, 128 MFLOPS, 92 SPEC-marks	RISC, MIPS R3000	Unix V.3	MIPS R3010 on CPU board	C: 128K R: 32–512M	760M, SCSI (1.6GB, SCSI)	S	N.A.	Custom	C: 19 in., 1024 × 1280	E, RS2, C, (Ultranet)	Multiprocessor configurations, license includes arbiter chip that allows access to custom system bus
Sun Microsystems Inc., SparcStation $14 995-$49 995, 30 days											
28.5 MIPS, 4.2 MFLOPS, 21 SPEC-marks	RISC, SunSparc	SunOS 4.1.1	On CPU board	C: 64K R: 16–96M	207M	N.A.	N.A.	N.A.	M: 19 in., 1024 × 864 (C: 21 in., 1280 × 1024)	E, TR, C, (FDDI)	Optional file server, database server, and print server
Tangent Computer Inc., M433I, $5290, 2 weeks											
15.01 MIPS, 1.0–25.0 MFLOPS (with Intel i860)	CISC, Intel 80486	MS-DOS 3.3 or 4.0 (Unix)	Weitek 4167-33 or Intel i860 on CPU board	C: 128K, 15 ns R: 4–32M, 70 ns	100M, IDE	0	0	VGA	C: 14 in., 1024 × 768	(E), (TR), RS2, (RS4), C	Options: 20-in. high-resolution monitor, larger hard drive, more memory, extra floppies
Tatung Science & Technology Inc., TWS-5020, $6995-$8495, 7 days											
12.5 MIPS, 1.4 MFLOPS, 8.3 SPEC-marks	RISC, LSI Logic 64801	SparcOS 1.1	Weitek 3170 on CPU board	C: 64K, 25 ns R: 8–64M, 100 ns	(207M, SCSI)	N.A.	N.A.	Custom	C: 19 in., 1280 × 1024 (1152 × 900)	E, RS2, (C)	
TeleCAD, Rocket Model 433I, $3200-$5800, 7 days											
14.5 MIPS	CISC, Intel 80486	MS-DOS 3.3 or 4.01 (Unix, OS/2, Novell)	On CPU chip	C: 64K, 15 ns R: 4–64M, 80 ns	(40–650M, IDE, ESDI, SCSI)	0	0	VGA	(C: 19 in., 1280 × 1024) (C: 16 in., 1024 × 768 or 1280 × 1024)	(E), (TR), RS2, (RS4)	64K cache is expandable to 256K second-level mapped cache
TeleVideo Systems Inc., Tele486Te, $9995-$15 000+, stock											
14.2 MIPS	CISC, Intel 80486	MS-DOS 4.0 (OS/2, Novell, Unix)	Weitek 4167 on CPU board	C: 128–256K R: 4–64M, 80 ns	200M, SCSI (80–150M, IDE, ESDI)	N.A.	N.A.	VGA	C: 14 in., 640 × 480	(E), RS2, C	
Twinhead International Corp., Twin-Station 1, $4500, 6 weeks											
12.5 MIPS, 1.2 MFLOPS	RISC, LSI Logic L64804	SunOS 4.1	N.A.	C: 64K, 25 ns R: 8–40M, 100 ns	213M, SCSI	N.A.	N.A.	N.A.	N.A.	E, RS2	Options: internal hard disk up to 400M bytes, 2.44M-byte 3-1/2-in. floppy-disk drive
Visual Information Technologies Inc., VITec 50 Image Computer, $39 900											
18 MFLOPS, 300 MOPS	RISC, custom	SunOS 4.1.1	On CPU board	R: 8–72M, 150 ns	N.A.	N.A.	N.A.	Custom	C: 19 in., 1280 × 1024	N.A.	
Wyse Technology Inc., Decision 486/33E, $11 999-$13 399, 4 weeks											
27 MIPS	CISC, Intel 80486	MS-DOS 4.01, (OS/2, SCO Unix)	On CPU chip	C: 128K, 15 ns R: 2–192M, 80 ns	300M, ESDI (660M, ESDI)	N.A.	N.A.	(VGA)	(C: 14 in., 1024 × 768)	(E), (TR), RS2, (RS4), (I48), C	128K-byte copyback cache, 64-bit-wide system bus

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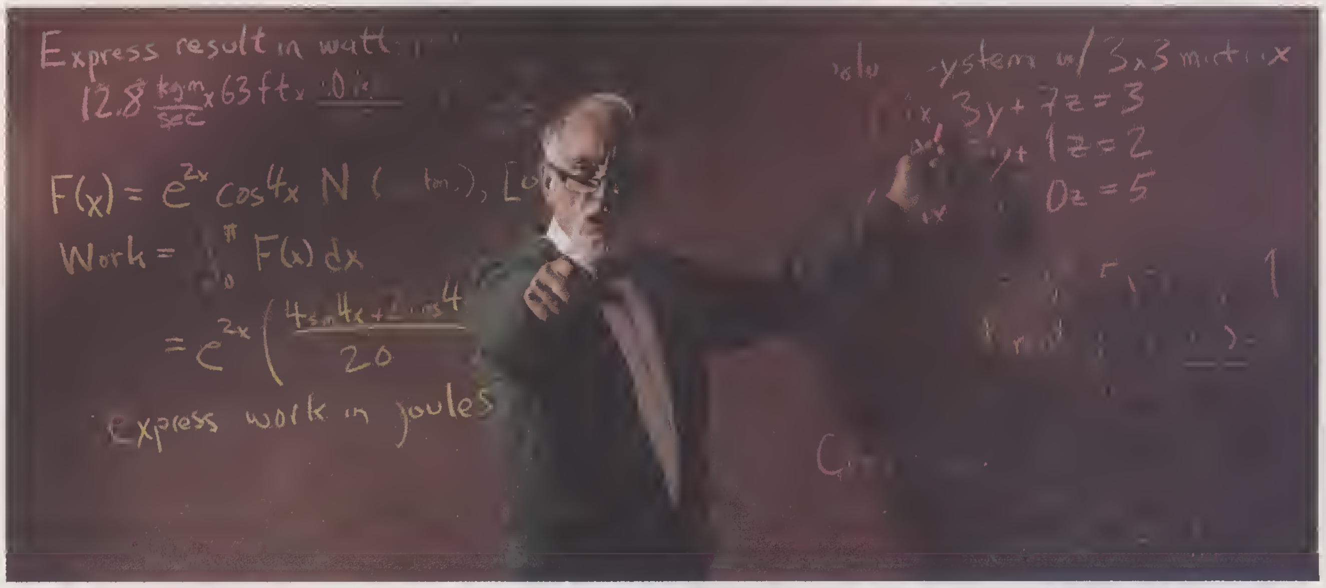

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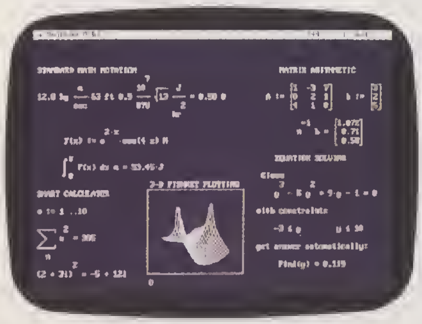

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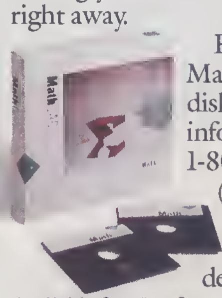

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Circle No. 215

(Continued from p. 39)
vironment, the Grumman CAD/CAM environment had grown to be very large and sophisticated. The large number of Catia and Cadam users performing complex tasks could strain the mainframe environment. The response time that the users experienced was not consistent and sometimes became unacceptably slow.

In the new workstation environment, in contrast, the user is isolated in many ways from the computer operations generated by the neighboring users. The result is that the workstation user experiences acceptable response time across the spectrum of functions and, even more important, consistent response time.

Another major problem was that the resources available in Grumman's mainframe environment limited the CAD/CAM model sizes, which in turn restricted designers' productivity. Because aerospace products are so complex, the limited model size constrained the ability to represent major components of the product in a single model. The workstation can provide more resources per user, enabling the allocation of larger model sizes without affecting other people on the network. This enhances productivity. Engineering, manufacturing, and quality assurance personnel operate more effectively because they can work with larger and more logical chunks of the design at one time.

The workstation environment also provides a more reliable system. On the rare occasions when a mainframe or the network went down, the entire user community was unable to work. However, in the distributed environment, even if the network goes down, the user can continue to work in a stand-alone mode.

A further workstation advantage is the ability to cost-effectively satisfy certain security requirements. This is achieved by isolating the workstations and tailoring their number for specific project requirements.

Another facet of Grumman's business is the fluctuation of requirements for CAD/CAM resources. As projects build up or slow down, it is necessary to adjust the allocations of computing resources. It is financially painful when the additional requirements force the acquisition of an additional mainframe. In the distributed environment, the company is protected from financial impact of increased computing requirements.

COMING TOGETHER. An integrated electronic design system is now possible with the advent of lower-cost, high-powered workstations operating in an open-architecture environment. This new hardware capability will enable Grumman to more fully establish an integrated workstation migration plan for the ECAD environment. The division is currently evaluating hardware and software operating within the overall distributed environment in order to accomplish full ECAD integration.

The plan will embrace the principles of standardization, as well as guarantee the independence of the hardware platform and the engineering application software. It defines a focused workstation strategy that is dynamic enough to change with the introduction of new technology, yet flexible enough in order to meet the rigorous customer-related requirements that are found in the aerospace industry.

Software functionality must be such that the application code is capable of being moved from one vendor's machine to another if required. The Grumman strategy is to implement software systems that can operate in a heterogenous hardware environment. It is therefore necessary to identify those systems that best fit this strategy—no special CAD operating systems layered over a standard operating system, nor special graphics accelerators, display units, or controllers will be employed, so far as possible. For ECAD, the engineering application software must support the concepts of the single-part database and neutral data formats. Consistent with Grumman's overall CIE implementation, compliance with standards (for example, Computer-Aided Acquisition and Logistic Support—CALS) is a must.

The programming environment will support higher-level languages and facilitate the
(Continued on p. 66)

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Add-ons for your workstation

There is a wide range of subsystems and add-on boards that can turn even the simplest computers into powerful tools

The world of workstations offers an embarrassment of riches. Not only are there scores of machines to choose from, but suppliers (such as those listed in the preceding article) offer a cornucopia of configurations and options. Then, too, the technology in workstation subsystems is constantly improving, so it's a rare system that isn't updated during its working life.

Before ordering or upgrading a system, the user should be aware of just what is needed to provide the desired capabilities. Given the vast range of choices, this is not a simple task. So it is necessary to look at the various classes of options and decide if they can actually deliver whatever is needed.

Customers can often return to the original vendor to find the kind of performance improvements they seek, and typically this is their first avenue of investigation. However, many third parties offer peripherals and boards that will increase system performance. These products can be attractive because they provide capabilities beyond those supported by the workstation maker or offer equivalent capabilities at a discount.

The table accompanying this article lists a representative sample of products that meet these criteria. As can be seen from the list, the number of products that enhance performance of a PC-based workstation currently outnumber those for other workstations, particularly those with a closed environment. But the latter are beginning to increase, and users should keep their eyes open for more third-party support as a particular workstation brand gains ascendency.

A workstation's central processing unit (CPU) is a general-purpose computing device that has its hands full acting as a manager of workstation functions. If this CPU has to take on a numerically intense task, like calculating the effects of various combinations of logic states for a very large-scale integrated circuit, an engineer waiting for the results will begin to feel that the workstation has decided to take a sabbatical.

Spectrum staff

A HELPING HAND. To avoid such roadblocks, workstations can be fitted with coprocessors or accelerators that take over specific types of functions. For example, a simulation coprocessor can take on the task of verifying logic layouts or checking for fault conditions, letting the main CPU simply manage the overhead of related data transfers while performing other tasks. In other cases, a coprocessor may change the nature of a system, adding the capability to use a reduced-instruction-set CPU in a PC based on a complex-instruction-set processor.

Because so many engineering tasks are mathematically intense, the most common add-on processor for computer-aided engineering (CAE) applications is the floating-point, or math, coprocessor, to which the CPU turns over the task of solving complex algebraic and trigonometric functions.

Such a coprocessor works with floating-point numbers, and workstation performance specifications given in millions of floating-point operations per second (MFLOPS) essentially reflect the power of these chips. Floating-point coprocessors are often standard equipment on high-end workstations such as HP/Apollos and Suns. Since the 80486 and 68040 microprocessors have built-in coprocessors, the newest high-end personal computers also have powerful number-crunching abilities. However, PCs based on the 80386 or 68030 do not necessarily come with math coprocessors; to run engineering applications comfortably on them will undoubtedly require a coprocessor.

However, adding a math coprocessor does not necessarily answer all speed problems. While such chips perform floating-point calculations as much as 10 times faster than the general-purpose CPU, all applications have other overhead functions that may, in fact, take up the most CPU time. For instance, a spread-sheet analysis's running time usually depends more on memory addressing than actual math. A math coprocessor will not speed up transfers between disk and memory, so it may prove equally important to make sure there is plenty of memory in the system so as to reduce the amount of disk swapping.

Few organizations want their workstations to be separate islands. Most want them to be connected with other systems with which they can share information, off-load complex jobs, or provide necessary control. For that reason, there is a brisk market in interfaces and adapters for workstations.

Most corporate locations are being wired for some type of local-area network (LAN) based on several of the 802.X standards. As a result, there are LAN boards available for Tbase2/5/10 types of networks that will work with any popular workstation. In addition, Fiber-Distributed Data-Interface (FDDI) boards are also beginning to appear. And, since design work tends to be data intensive, it is not surprising to find many boards that will connect workstations to SCSI-compatible storage peripherals. Other boards let workstations communicate over the IEEE-488 bus. Not only will this permit the addition of storage devices and digitizing scanners, but it will also allow the system to control measurement systems and instrumentation.

Even if a workstation has no other interface, it will have a graphics adapter, whose function it is to send data to a display. It is the graphics adapter that determines with what

(Continued on p. 56)

Folsom Research Inc.

The latest addition to workstation peripherals, special video systems let users capture on-screen operations and transfer them to videotape, which can be used later for both employee training and sales presentations.

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Representative sample of add-on boards and peripherals for workstations

Company	Product	Year first available	Unit cost (US $)	Key specifications	Features and comments
Hardware accelerators and coprocessors					
Alacron Inc.	AL860 AT	1990	$6395 (33 MHz)	40-MHz i860 with 2M–16M bytes, 40 MIPS, 80 MFLDPS	Available in AT- and VMEbus-compatible versions, can add 2 daughter boards, e.g. 24M-byte RAM, SCSI
Avalon Computer Systems Inc.	Vaccelerator AP/30	1990	$15 900	33-MHz MC88100, 33 MFLDPS	Q-bus- or Unibus-compatible, multiple 16K-byte cache, 256M-byte 80-ns dynamic RAM
Computer System Architects	SuperSet Plus 16FP	1990	$17 640	16 20-MHz 32-bit I800 transputer	PC and Sun models, 1M byte per CPU/FPU, can be organized as mesh or hypercube by user
Infotek Systems	DSP332	1990	$2900	WE-DSP32C, 15 MFLDPS	Compatible with HP workstations with DID bus, includes HP Basic Applications kit
Intel Corp.	387 DX-33	1989	$994	33 MHz, 32- to 80-bit data, for floating-point math	IC, compatible with 386 CPU, fits PC FPU socket, 1.0-μm technology, low power
Loughborough Sound Images Ltd.	SDSP/C30	April 1991	$2995	TMS320C30, 33 MFLDPS	Compatible with Sun Sbus, 1M-byte 25-ns static RAM, 8K-byte video RAM, analog I/D and SCSI Interface included
Mercury Computer Systems Inc.	MC860	1990	$8900 base	40-MHz i860 with 16M bytes, 40 MIPS, 80 MFLDPS	VMEbus-compatible, one-slot, multitasking, board-configurable, 450-algorithm library
MicroWay Inc.	Number Smasher-860	1990	$9200	40-MHz i860 with 8M bytes; 80 MFLDPS, 4–8 Linpacks	Compatible with 80286/386/486, includes compiler for DDS, Xenix, Unix, and SunDS, supports transputer nets
Dpus Systems	500-C Personal Mainframe	Jan. 1991	$7195	LSI Sparc, 12.5 MIPS, 1.4 MFLDPS, 10.0 SPECmarks	Compatible with AT bus, runs SunDS and works in parallel with 80x86, gives DDS window
Sky Computers Inc.	Skybolt	1989	$12 000	40-MHz i860 and i960, 2M–16M-bytes, 40 MIPS, 80 MFLDPS	VMEbus-compatible, one slot, static RAM cache, software for automatic vectorizing available, 54-Mb/s expansion port
Torque Computer Inc.	Compute Server d1	1990	$18 500	Up to 1 GFLDPS, peak	Network computational server, scalable up to 16 i860 processors
Zycad Corp.	XP-100	1990	$40 000	Custom, 1000 MIPS	Logic- and fault-simulation accelerator compatible with VME, AT, and Sbus, includes EDIF library
Interface and adapter boards					
Local-area networks					
Interphase Corp.	V/FDDI 4211 Peregrine	1990	$8995	100 Mb/s	VMEbus-compatible, RISC-based 6U node processor for FDDI
Milan Technology Corp.	Micro-Mau Mil-02T	1990	$149	10 Mb/s	Ethernet for workstations, connects directly to any AUI connector
3Com Corp.	Etherlink 16	1990	$445	10 Mb/s	Ethernet card for PCs and compatibles, 8-/16-bit self-adapting bus interface
Western Digital Corp.	EtherCard Plus Elite 16 Combo	Jan. 1991	$399	10 Mb/s	Ethernet card for non-Microchannel PCs, one jumper selects 10Base 5, 10Base 2, other configurations
Interfaces					
Antares Microsystems Inc.	SC-320	1990	$395	38.4 kbaud	8-channel serial interface for Sun Sbus, each channel programmable, full modem support
Interphase Corp.	E/SCSI 4810	1990	$2995	33M-byte/s burst mode	32-bit EISA bus-master SCSI interface, configurable with single or dual ports, supports up to 14 devices
Iotech Inc.	SB488	1990	$995	1-Mbyte/s read/write	IEEE-488 interface for Sun Sparcstation 1, 1+, and IPC, includes device driver and language interface
Macrolink Inc.	VMEbus Multiplexor MVC/16	1990	$2395	38.4 kbaud	16-port asynchronous communications multiplexer for VMEbus, serial-port and bus parameters programmable
National Instruments Corp.	GPIB-SPARC1-B	1990	$995	1M-byte/s read/write	IEEE-488 interface board for Sparcstation 1, includes multitasking SunDS software and development utilities
Solflower Computer Inc.	SFVME-300	1900	$2895	20M-byte/s VMEbus burst mode	Sun-to-VMEbus converter, compatible with Sun 4 device drivers
Graphics adapters					
Acer/Altos	VGA1024	April 1991	$189	1024 x 768 pixels noninterlaced	VGA-, PC-compatible
ATI Technologies Inc.	8514/Ultra	Feb. 1991	$599–$799	1024 x 768 pixels, 70-Hz refresh rate	PC AT-compatible, up to 10 times faster than 8514/A, screen resolution as high as 300 dots per inch
Cardinal Technologies Inc.	VGA700/ 1MB	1990	$269	1024 x 768 pixels, 8 bits/pixel	PC-compatible, includes 8514AI driver
RasterDps Corp.	24L Display System	1990	$8190	1024 x 768 pixels, 24 bits/pixel	Macintosh II-compatible, includes 19-in. Trinitron monitor
Spectre Corp.	SP300	Feb. 1991	$9000	1280 x 1024 pixels, 32 bits/pixel	AT-compatible with TI34020 graphics engine, 8M-byte video RAM, expandable to 1600 x 1200 pixels

Workstation add-on boards and peripherals (continued)

Company	Product	Year first available	Unit cost (US $)	Key specifications	Features and comments
Storage and backup systems					
Memory boards					
Dataram Corp.	DR-5000	1990	$18 000	480M-byte capacity	For DECstation 5000 workstations and DECsystem 5000 servers
Helios Systems Division of Piiceon Inc.	MHP400	Jan. 1991	N.A.	32M-byte capacity, 80-ns access time	For HP Series 400 workstation
Infotek Systems	EM400	1990	$2000	32M-byte capacity, 80-ns access time	For HP Series 400 workstation
Micron Technology Inc.	Xceed IIci-128	1990	$419	128K bytes	Cache card for Macintosh IIci, static RAM cache returns data in under 30 ns
Parity Systems Inc.	4/330 Expansion	1990	$1365	8M bytes	For Sun 4/330, versions to 32M-bytes
Tecmar Inc.	MicroRam 386	1989	$549 plus $100/Mbyte	0–32M bytes	Microchannel architecture, for PS/2 models, zero wait state
Disk emulators					
Cardinal Technologies Inc.	FlashCard/RC1100F	1990	$199	2M bytes	PC-compatible, includes DR-DOS 5.0 in RDM, electrically reprogrammable flash memory
Macrolink Inc.	Solid-State Disk v/SSO	1985	$10 500	32M bytes, 10M-byte/s data rate	VMEbus-compatible solid-state disk, expandable to 256M bytes, 1-ns average access time
Western Automation Laboratories Inc.	Ramstor 5150	1988	$3495	0.5-ms access time, 5M-byte/s data rate	SCSI-compatible systems, 5-1/4-in. form factor, optional battery backup, expandable to 320M bytes
Magnetic-disk drives					
Conner Peripherals Inc.	CP3500 Summit	1990	N.A.	510M bytes, 2M-byte/s data rate	3.5-in. drive in PC/AT and SCSI models
Infotek Systems	MS660	1990	$5995	600M bytes, 4M-byte/s data rate	For HP 9000 300/400, Sun 360 and Sparc 1 workstations, digital-audio tape (DAT) backup optional, upgradable to 1.6G bytes
Iomega Corp.	Bernoulli Transportable 44	1990	$1259	44.5M bytes	Compatible with MS-DDS, OS2, and MacOs, portable or dual unit available
Maxtor Corp.	LXT-535	1990	N.A.	535M bytes, 20.5M-b/s data rate	Either embedded SCSI or AT controller, 437M-byte version available
MegaDrive Systems Inc.	MegaOrive P425	March 1991	$4599	426M bytes	Compatible with MS-DOS, DS/2, Windows, Unix/Xerox, and MacOS, removable drive system
Micropolis Corp.	HS Drive 1684	1990	$1865	380M bytes, 4-Mbyte/s data rate	3.9-ms effective access time, SCSI interface, half-height form-factor
Parity Systems Inc.	PS5100	1988	$2290	327M bytes	For Sun, IBM RS6000, Silicon Graphics, and Solbourne systems, models available with tape/floppy drives
Plus Development Corp.	Impulse	1990	$700	209M bytes, 4M-byte/s data rate	SCSI-compatible; available in 120M-, 168M-, and 425M-byte versions
Seagate Technology Inc.	Sabre PTO ST82105K	1990	$25 000	2.1G bytes, 24M-byte/s data rate	Reads and writes with 8 heads in parallel, 9-head version available, IPI-to-VME controller standard
SyQuest Technology	SQ5110	1990	$1000	88M bytes, 32M-b/s data rate	Removable cartridges, integrated SCSI controller, half-height 5.25-in. form factor
Erasable optical drives					
Iomega Corp.	LaserSafe	N.A.	$4999	652M bytes, 5.5M-byte/s data rate	Supports DS/2 and MacOS, 256K-byte dual-port cache
Laser Magnetic Storage International Corp.	Laser Orive	1990	$4000	653M bytes per disc; 490K-byte/s data rate	Multicartridge/autochange optional, integrated SCSI controller
Write-once, read-many drives					
Literal Corp.	525GB	1991	$4399–$4899	1.3G bytes per cartridge	Internal and external configurations, dual-drive system available
Sony Corp.	WOO-600 Writable Disk Drive	1989	N.A.	4.36–6.55G bytes, depending on disk model	Autochanger can extend capacity to 328G bytes per drive, seven drives may be daisy-chained to provide 2.29T bytes
Compact-disc ROM					
NEC Technologies Inc.	Intersect CDR-83/73	Feb. 1991	$849/$949	200M–680M bytes	External or internal model compatible with PCs, PS/2s, and MACs
Winchester Technology	WT-S-241 Oisc and Tape Subsystem	1990	$3100	1.2G-byte disc subsystem	SCSI-based, compatible with Sun, IBM/RISC, and Mac

Workstation add-on boards and peripherals (continued)

Company	Product	Year first available	Unit cost (US $)	Key specifications	Features and comments
Tape systems					
Alloy Computer Products Inc.	Retriever/ 2200	1990	$7995	2.5G bytes per 8-mm cartridge	Compatible with Banyan, PC-LAN, 3-CDM, or stand-alone machines, has SCSI controller, software for scheduled unattended backup
Emerald Systems Corp.	Rapid Re-cover 1.3GB	1990	$7290	1.3G bytes	Compatible with NetWare 386 file server, EmQ software included lets multiple tape drives be installed
Irwin Magnetic Systems Inc.	Model 9231 SE	1990	$6896	4.6G bytes per 8-mm cartridge with data comparison	SCSI-based, compatible with PC XT/AT and PS/2, 0OS, and SCO Unix, automatic backup
Mountain Network Solutions Inc.	FileSafe 1200	1990	$5995	1.3G bytes per cassette; 183K-byte/s data rate	Oigital-audio tape (DAT) technology, maximum capacity is 3.2G bytes in 2 dual-drive units, standalone or half-height form-factor internal
Palindrome Corp.	Fast 1300 Series TS-F1300-A	1989	$4995	1.3G bytes per cassette, 183K-byte/s data rate	OAT technology, for PC/AT, includes software for protecting up to 350M-byte disk, expandable
Sysgen Inc.	Maxi DS/2 TS1300	Jan. 1991	$5785	1.3G bytes, 183K-byte/s data rate	OAT technology, for OS/2 Law Manager
Tallgrass Technologies Corp.	File Secure FS4000	1989	$4595	2.2G bytes, 10M-byte/minute data rate	OAT technology with data compression, supports MS-0OS, OS/2, Novell, Unix, and MacDS, SCSI interface
Wangtek Inc.	5525 SCSI Tape Orive	1990	$1195	525M bytes	Compatible with Q1C-150,-120, and -24 formats, 1G-byte unit available
Input devices					
Mice					
Kye International/Genius	Genius GM-F303	1989	$109	125–1400-dot/in. resolution	Resolution selectable by button or software, optical encoder/steel ball technology, PC- and PS/2-compatible
Logitech Inc.	Cordless Radio MouseMan	Jan. 1991	$199	400-dot/in. resolution	Radio-transmission mouse, user frequency-selectable (8 choices), one-year battery life
Mouse Systems Corp.	PC Mouse III	1990	$169.95	30–30 000-dot/in. resolution	Resolution selectable by button or software, 100% optical technology, accurate to within 0.001%
Track balls					
Kensington Microware Ltd.	Expert Mouse 2.0	1990	$149.95	200-dot/in. resolution	2-button trackball with click-lock and chording features, PC- and PS/2-compatible, bus and Windows 3.0 driver versions available
MicroSpeed Inc.	PC-Trac	1990	$119	50–1000-dot/in. resolution	PC- and PS/2-compatible; includes driver for Auto-Cad, bus version available
Digitizer tablets					
Altek Corp.	Datatab Oigitizer Series	1978	$1300 for 12-in.-sq model	0.001-in. resolution	0.07-mm accuracy, table range: 12 in. sq. to 60 by 120 in., backlit opaque or rear-projection styles
GTCO Corp.	GTCD Super 1987 L Series	$1695–$3995	N.A.	0.001-in. resolution	Other resolutions selectable, PC-compatible, sizes 17 by 24 in. to 42 by 60 in.
Hitachi America Ltd.	Puma Plus/ HOG-1212E	1990	$549	1016-line/in. resolution	0.020-in. accuracy, supports over 250 CAD/CAE packages, compatible with PC, Sparcstation, and Decstation
Kurta Corp.	XLC2436 Oigltizer	1990	$3795	1279-dot/in. resolution	0.005-in. accuracy, 24 by 36 in., dual pen/cursor ports, template programmability
Numonics Corp.	Grid Master	1989	$449–$469	1000-line/in. resolution	0.010-in. accuracy, 1/32-in.-thick flexible digitizer pad rolls up for storage, pen-tilt correction, PC- and MAC-compatible
Science Accessories Corp.	GP-9 Sonic Oigitizer	1990	$2195	1000-line/in. resolution	No special work surface required, 27 by 7 in., PC- and workstation-compatible, emulates any digitizer format
Scriptel Corp.	ROT 12x12-in.	1988	$1295	1000-line/in. resolution	Transparent surface, 0.010-in. accuracy, other sizes to 24 by 36 in., emulates Summagraphics, and others
Summagraphics Corp.	Summa Sketch II	1989	$599	1016-line/in. resolution	0.015-in. accuracy, PC-compatible, 11.7 in. sq., 350 applications, templates for AutoCad, VersaCad, and Animator
Wacom Inc.	S0-510	1989	$695	508-line/in. resolution	Cordless, batteryless, 0.020-in. accuracy; 6 by 9 in. (larger sizes available), Macintosh-compatible
Output systems					
Monitors					
NEC Technologies Inc.	MultiSync 5D Color Monitor	1989	$3699	20 in., 1280 by 1024 pixels	Color, dynamic beam focus and dual focus, digital controls
Radius Inc.	TPD/PC	1990	$2590	21 in., 1280 by 960 pixels	Grayscale/paperwhite, includes interface card, high-speed drivers for Windows 3.0, VTGA-, PC- and PS/2-compatible

Workstation add-on boards and peripherals (continued)

Company	Product	Year first available	Unit cost (US $)	Key specifications	Features and comments
Tatung Co. of America Inc.	CM-2020	April 1991	$3399	20 in., 1280 by 1024 pixels	Color, dynamic focusing, VGA-, Super VGA-, Macintosh II- and Sparcstation 1-compatible
Wyse Technology	WY-890N	1989	$2899	19 in., 1024 by 768 pixels	Color, noninterlaced video refresh, OCLI antiglare coating
Scan converters					
Folsom Research Inc.	Video/Scan 9100	Jan. 1991	$13 900	N.A.	Video scan converter and frame grabber for IBM RS 6000, 24-bit frame buffer
RGB Technology Inc.	RGB/Video-link 1450	Feb. 1991	$14 995	20–80-MHz horizontal scan rate	Real-time video scan conversion for videotaping, autosync, compatible with workstations, PCs, and Mac IIs
Graphics printers					
Fujitsu America Inc.	DL4600	1990	$1395	N.A.	Supports Sun's Newsprint software, handles multiple paper types and sizes
Okidata Group of Oki America Inc.	OL840 LED Page Printer	1990	$2999	N.A.	Laser PostScript printer, software-selectable emulations and interfaces for multi-environment offices
QMS Inc.	PS-410	1990	$2795	N.A.	Includes PostScript, simultaneous interface operation (serial, parallel, AppleTalk), also provides automatic emulation switching
Tektronix Inc.	Phaser II PXN	Jan. 1991	$2995–$10 995	300-dot/in. resolution	Thermal-wax color printer, PostScript-compatible, 3 ports (Centronics, RS-232, AppleTalk) plus Ethernet
Plotters					
CalComp Inc.	Drawing Master Plus (52436)	Jan. 1991	$22 995	406-dot/in. resolution	High-speed toner-free raster plotting, includes 4-to-1 input multiplexer and two-color (black and red) capability
Houston Instrument Co.	DMP-61 DL	1989	$4895	Plotting speed up to 45 in./s (diagonal)	0.0005-in. mechanical resolution, system capabilities include pen and vector sorting, Quick scale feature

(Continued from p. 52)
resolution, given in terms of horizontal and vertical pixels, a system can display data.

At critical times in a project, it always seems that the quantity of memory needed exceeds the quantity available. Sooner or later, then, extra memory must be added to the system. Enlarging internal RAM can also make an application run faster, since less time is spent moving between disk storage and the RAM.

Similarly, adding cache memory (if system design permits) raises performance by using faster RAM to supply immediate processing requirements. But critical to the performance increase is the cache miss rate; that is, how likely it is that data will not actually be in cache when needed. If the data required cannot be scheduled into cache according to some fairly reliable algorithm, then expanding the expensive, high-speed cache does not buy much improvement in performance.

Most workstations come with hard-disk drives, and the cost per bit of these drives is constantly decreasing. That makes it highly likely that at some time in its life a workstation drive will be upgraded to a higher-capacity unit. Further, some disk-drive systems allow users to add additional hard-disk capacity as their need for storage increases without swapping out the previous drive or changing the drive controller. Of course, users should know just how much disk storage, internal or external, their system can support.

Some workstation manufacturers have taken to offering compact-disc ROM (CD-ROM) drives as options on their newest models, because the compact disc is becoming a popular way of distributing large engineering applications and extensive software libraries. Current workstation users can also turn to third-party suppliers. Because of its density, digital audio tape (DAT) is also being considered as a distribution medium, as well as a back-up option.

In fact, there is an ocean of options for backing up design information, from reels of half-inch tape to write-once/read-many (WORM) cartridges. Choosing the right type depends on a company's requirements. A typical scenario is one in which data is backed up once a week for everyone, but for critical projects, data may need to be backed up daily or even more frequently.

In choosing a back-up approach, a company needs to examine its operations and establish policies to which everyone adheres. One of the first questions a company should answer is, "Do we always need to have immediate access to backed-up data?" If the answer is yes, a company has essentially three choices: floppy drives, fixed hard drives, and removable-disk-cartridge drives. On the other hand, if, in the event of data loss, a company can re-install backed-up data at a more leisurely pace, there are optical- and magnetic-tape systems that will fill the bill.

OF MICE AND KEYS. The typewriter-style keyboard is still the primary means of interacting with a workstation. The kind of keyboard required in a particular environment depends upon the kind of network operations performed. For example, VT220-style keyboards will often be required in facilities that have grown up around Digital Equipment Corp. machines, particularly if the workstation happens to be part of an X Window System environment. Further, some keyboards have other types of manual-interface technology, such as a trackball, built in. If a trackball is one of the preferred manual devices, then such a keyboard will save space on the desktop.

Still, the mouse is undoubtedly the second most popular manual device with workstations, and the technology keeps on improving. For one thing, mice vendors are beginning to offer left-handed devices. Also, whereas all older mice had to be connected to workstations by cables, units are now beginning to appear that use infrared (IR) or radio frequency (RF) signals to communicate with the workstation's main housing.

Many users will be glad to become untangled from their system, but they need to investigate whether the cable-free devices will work in their environments. IR systems, for instance, will require a clear line-of-sight to the input port on the workstation, and if there are too many RF broadcasting mice in the area, users could be manipulating data on other systems.

The popularity of the mouse has overshadowed earlier technologies, such as the trackball and the light pen, but these too have advanced. Trackballs are attractive on desktops where space is at a premium; they do not require a "mousing area" or mouse pad to operate. They also give an operator very fine control over the position of the cursor on screen as well as allowing the cursor

to be positioned very quickly. However, they typically require two separate hand movements: the operator first moves the track ball and then hits a cursor-activation key. In contrast, a mouse provides cursor positioning and activation without repositioning the hand.

Since drawing with a stylus is natural, many digitizer tablets now support this input method too. The digitizer stylus operates like a mouse; the operator points to the digitizing pad and clicks a button on the stylus to start drawing.

In addition to operating with the stylus, digitizing pads can be used with a "puck"—a mouse-like device with a set of cross hairs that can be placed over a specific point to be captured. The puck makes it easy to copy existing drawings or sketches into an electronic format.

Several digitizer manufacturers offer templates for electronic engineering. These templates have standard electronic symbols, such as AND and OR gates, on the perimeter of the drawing area. By simply pointing to them, the user avoids having to draw the symbol each time it is needed. Software installed with the digitizer is designed to support the particular template; this also permits customization of templates in several cases.

For a typical workstation environment, an engineer will want a digitizer that fits comfortably on a desktop. For creating complex engineering drawings, there are digitizers as large as a drafting table, and ones that actually include a table.

THE BIG PICTURE. For workstation users, the monitor is the primary source of information. Since users spend a good part of the day in front of a screen, the monitor should provide a quality display that enhances their ability to work and will not harm them. Obviously, getting the most out of a monitor depends upon using an appropriate graphics adapter, as previously discussed.

When given a screen's diagonal as a specification, it is best to clarify what the manufacturer is actually defining. Not all the area of the CRT's face is typically used for display since curvature can cause distortion. So on a tube that measures 20 in. on the diagonal, the actual display area may be 19 in. diagonally.

Since users should be able to view a screen comfortably from about 75 centimeters away, those who spend a lot of time working with it will want at least a 17-in. display, and if they expect to display complex graphics and schematics they may insist on 19-in. or larger screens.

A more common way of capturing information today is on paper. For report generation, only a simple black-on-white printer may be needed. A good-resolution printer can usually be found discounted for under $1000. Full-color printers can be an order of magnitude more expensive, and therefore it makes sense to set them up as a shared network resource. ◆

How ICs impact workstations

Start with a wide choice of IC technologies, then break the rules for system architectures, and reap price/performance benefits

Editor's note: The following article describes the design process employed by a group of Hewlett-Packard workstation designers in creating a prototype for a high-performance, low-cost workstation, and how performance goals and design capabilities influenced decisions about what types of ICs should be used. While the performance results presented for the prototype are exceptional, the purpose of this article is to explore the decision-making process.

In the recent design of a new family of advanced workstations, a team of design engineers took on the task of moving an existing architecture—the Precision-Architecture, Reduced-Instruction-Set Computer (PA-RISC) design—into the realm of a low-cost desktop computer. The PA-RISC, in use since 1986, was initially employed primarily for multiuser and commercial computing applications. The goal of this design effort (begun in 1989) was to make a PA-RISC implementation suitable for a high-performance single-user workstation that would provide exceptional application and graphics performance, yet would also provide continuity with existing systems.

The design team resolved that the system should support I/O expansion with an industry-standard bus, which would allow users to take advantage of widely available add-in cards and peripherals. This would also allow the design team to concentrate on other areas, where innovation would provide the highest return in terms of cost and performance.

The team set about defining specifications for a system that would meet all these goals. Market researchers, as well as both internal and external customers, supplied inputs on what requirements needed to be met in order to provide the best value at the customer application level. A diverse team of technical experts in such areas as very large-scale integration (VLSI) design, system hardware design, compiler technology, operating systems, performance analysis, graphics subsystems, and manufacturing reviewed these inputs and defined the system architecture and technology requirements to optimally meet the performance, cost, and schedule goals.

Together, these experts explored both traditional and nontraditional approaches to workstation architectures. A unified system-level design approach, which emphasizes rethinking the design of each component or subsystem in terms of the global system needs and making appropriate tradeoffs between the various pieces, was adopted.

The design leverages many technical advances—in processor architecture, optimizing compilers, manufacturing techniques, graphics—not just those in ICs. The chip-selection strategy was unique in that the team had the flexibility, resources, and expertise to choose a combination of the best of all worlds: innovative full-custom designs for the components that define the machine's critical attributes and set it apart from designs based on off-the-shelf components, standard logic ICs to implement industry standard I/O functions, commodity chips for more cost-sensitive areas such as main memory and cache memory, and a variety of specialized application-specific ICs (ASICs), which combine numerous noncritical functions to reduce area and cost.

OVERVIEW. In the resulting architecture [Fig. 1], the core PA-RISC processor consists of a central processing unit (CPU), a floating-point coprocessor, and separate data and instruction caches. While designed to work as a single unit, the CPU is not a single IC. Contrary to popular design trends, the cache memory is not incorporated into a CPU IC, but rather it is built from off-the-shelf static RAMs. The CPU and coprocessor are separate ICs, rather than a single chip. Yet with these separate components designed into a tightly coupled processor, the system achieves the highest performance currently known for a RISC workstation; at a clock speed of 66 megahertz, it benchmarks at 72 SPECmarks overall (51 integer, 91 floating-point), 76 million instructions per second (dhrystone 1.1), 22 compiled, double-precision Linpack million floating-point operations per second, and 34 single-precision MFLOPS. This performance can be attributed to a unified design approach optimizing system timing, pipeline efficiency, cache memory size/speed, and bus structures, along with complementary advances in compiler optimization, system software, and instruction-set architecture extensions.

Key to using the CPU for a workstation is the custom VLSI memory and I/O controller IC that provides the critical high-speed link between the CPU, memory, I/O, and graphics subsystems. In another departure from conventional workstation architecture, advanced graphics acceleration logic is designed directly into the core of the memory and I/O controller IC (and supported by special processor instructions as well). These features were defined jointly by a group consisting of VLSI, graphics-hardware, and graphics-algorithm/-software designers—

Closely coupled engineering made it possible to design an inexpensive desktop workstation with an extended RISC architecture that yields extremely high performance.

Hewlett-Packard Co.

Robert J. Horning, Mark Forsyth, Jeff Yetter, and Larry J. Thayer
Hewlett-Packard Co., Fort Collins, Colo.

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Representative sample of ICs generally used in workstations

Company	Product	Available as of:	Unit cost (1000 qty., US $)	Key specifications	Features and comments
RISC microprocessors					
Advanced Micro Devices Inc.	AM29050	March 1991	$410	40 MHz 32 MIPS 80 MFLOPS	Floating-point unit and 1K-byte target cache on chip
Cypress/Ross Technology Inc.	CY7C601	1989	$805 (100s)	40 MHz 29 MIPS	Chip family includes floating-point unit, memory management unit, and cache static RAMs
					organized as 8 windows,
					ible
					lities for visualization and ren-
					agement units and cache con- ipport
					PS Computer Systems CPU, uction and data caches, and I/O
					ower
					laptop workstations
					ut external power, both memory
					0.7-μm, 2-layer metal CMOS
					Sparc MMU architecture, 256K- dressing
					ons, accelerates Windows 3.0
NCR Corp.	77C22E display controller	March 1991	$29	Color expansion	Motherboard interface for fast operation
Texas Instruments Inc.	TMS320-C30 DSP	1989	$137 (27 MHz)	220 MOPS (40 MHz)	Dual bus architecture for 3-D pipeline operations, 8K-byte RAM on chip
I/O					
National Semiconductor Corp.	DS38883/4/5/6, bus interface	March 1991	$8–$11 (100s)	Controlled rise times	5–10 times bus speed improvement over discrete TTL, low capacitance
Signetics Corp.	74ABTxxx bus interface logic	1990	$1.79–$8.53	4.6-ns worst-case buffer/transceiver delay	Uses advanced BiCMOS (QUBiC) process, less than 50-mA static power dissipation, +64-mA/–32-mA output current drive
Memory					
Hitachi America Ltd.	HM624256 AJP-20 1M-bit static RAM	1990	$135	20-ns access time	0.8-μm CMOS
Toshiba America Inc.	TC514100 4M-bit dynamic RAM	1990	$29	60-ns access time	300- and 350-mil SOJ packages

another example of the benefits of a unified, system-level design approach. Together they contribute to reducing the cost of high-performance graphics workstations. Moreover, along with the graphics software and add-in hardware, they allow the systems to deliver graphics benchmark performance of more than 1 million vectors per second, by far the highest in the industry for this class of machine.

The classic RISC design philosophy embodies more than just the set of instructions that a machine runs. From the hardware design perspective, it asserts that by keeping complexity to a minimum, a design can be made to run at higher speeds—thereby delivering higher performance at a lower cost (and shorter design schedule). Clock speed is the most important design parameter that needs to be optimized in RISC designs in order to deliver balanced, high performance on all applications. Higher frequencies improve performance linearly on nearly all computationally bound applications, whereas added features generally only improve performance on a smaller class of problems.

For the CPU design, the team set a goal of using a basic system clock with a frequency greater than 50 MHz. To meet this frequency goal, most engineers would look to emitter-coupled logic or gallium arsenide technology. But while these technologies could meet speed requirements without

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Editor's note
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Cypress/Ross Technology Inc.	CY7C601	1989	$805 (100s)	40 MHz 29 MIPS	Chip family includes floating-point unit, memory management unit, and cache static RAMs
Fujitsu Microelectronics Inc.	MB86903	March 1991	$350	40 MHz 29 MIPS 5 MFLOPS	On-chip floating-point unit, 136 registers organized as 8 windows, peripherals available
Integrated Device Technology Inc.	79R3000A	1990	$275 (100s)	40 MHz 33 MIPS 11 MFLOPS	MIPS architecture, plastic package available
Intel Corp.	i860	1989	$567	40 MHz 57.5 MIPS 10 MFLOPS	On-chip floating-point unit, includes facilities for visualization and rendering
Motorola Inc.	88100	1988	$150	33 MHz 28 MIPS 5.4 MFLOPS	Integer, floating-point, and memory management units and cache controller on chip, built-in multiprocessor support
Performance Semiconductor	PIMM	March 1991	$1300	40 MHz 33 MIPS	Single VLSI package contains 32-bit MIPS Computer Systems CPU, floating-point accelerator, 32K-byte instruction and data caches, and I/O
VLSI Technology Inc.	VL86C020	1989	$100	25 MHz	On-chip 4K-byte cache; CMOS for low power
CPU peripherals					
AT&T Microelectronics	V.32 modem chip set	March 1991	$70/3-chip set	9600 b/s, low power	Small footprint, for on-board modems in laptop workstations
Dallas Semiconductor Corp.	DS1387 real-time clock with RAM	1990	$13.79	4K-byte NV SRAM on chip	Keeps time for more than 10 years without external power, both memory and calendar functions
LSI Logic Corp.	L64811 Sparc integer unit	1990	$250 (100s)	40 MHz 29 MIPS	Executes most instructions in one cycle, 0.7-μm, 2-layer metal CMOS technology
Cypress/Ross Technology Inc.	CY7C605 cache controller/MMU	March 1991	N.A.	N.A.	Supports multiprocessing, conforms to Sparc MMU architecture, 256K-byte virtual cache, 64G-byte physical addressing
Graphics					
Chips & Technologies Inc.	PUMA	March 1991	$90	N.A.	Two-chip set for complex graphics functions, accelerates Windows 3.0 graphics applications and AutoCAD
NCR Corp.	77C22E display controller	March 1991	$29	Color expansion	Motherboard interface for fast operation
Texas Instruments Inc.	TMS320-C30 DSP	1989	$137 (27 MHz)	220 MOPS (40 MHz)	Dual bus architecture for 3-D pipeline operations, 8K-byte RAM on chip
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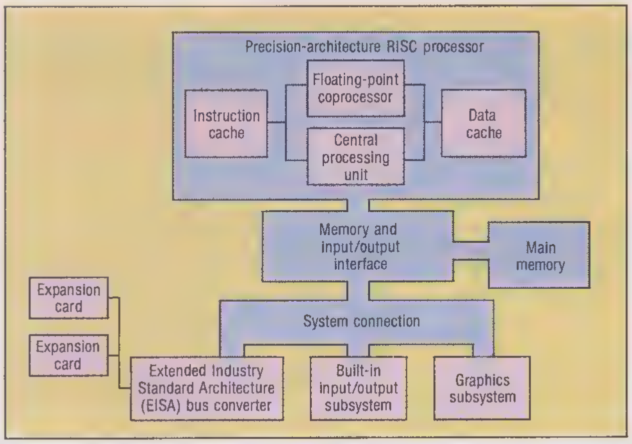


[1] The workstation under discussion can be divided into four systems: PA-RISC processor, memory, built-in I/O, and graphics. Its high performance is due both to the nontraditional, segmented design of the processor and to the system communication hub—the memory-I/O interface.

much effort, they are expensive, require a lot of power, and generate much heat, thereby increasing a workstation's cost. So, with the support of process engineering, the designers worked out CPU timing requirements in low-power CMOS technology, thus avoiding such penalties.

THE PROCESSOR ARCHITECTURE. In the design of the processor, the group faced some interesting choices. A key challenge for the RISC processor designers, with the variety of high-performance design techniques available, is in optimally matching the most appropriate technique with available fabrication technologies to best meet system performance and cost requirements. The team determined that a single-chip–processor implementation fabricated in today's production 0.8-to-1.0-micrometer technologies could not meet the aggressive performance requirements of this system. It would limit the maximum size of cache memories excessively and would offer limited silicon area for other functions such as multiple 64-bit floating-point functional units. Furthermore, the resulting complexity, die size, and density of the single-chip design would be inconsistent with schedule and manufacturability goals. They also limit flexibility of system designers to configure for operations at different cost and performance levels. The design team also determined that a lower-density, multichip design would lend itself to being able to quickly take advantage of future VLSI and static RAM evolution.

High levels of performance can also be achieved using separate ICs for the major CPU elements if the architecture is well thought out and its timing is well controlled. Conventional design philosophy today says that high clock frequencies can be achieved only with on-chip cache techniques—a theory proven untrue by the results of the design effort. Furthermore, as system performance levels increase, so does the size of typical customer applications. While single-chip designs can deliver impressive ratings on small benchmarks, the design team believed that typical applications on 50-MIPS-plus workstations would require much more muscle, particularly in terms of larger cache memory sizes, to be able to sustain the high performance in real user environments.

The PA-RISC processor is based on the use of two custom CMOS VLSI ICs. One is a 577 000-transistor integer unit built using an in-house, 1.0-μm-line-width process. The other is a 640 000-transistor floating-point coprocessor fabricated in an 0.8-μm process; this chip was designed jointly with Texas Instruments and produced using its EPIC-2 CMOS technology. Each chip is housed in a custom ceramic pin-grid-array package that was carefully designed to support both high-frequency operation and high signal-pin counts. With these packages the chips can operate at clock speeds of 66 MHz with up to 225 simultaneously switching output drivers (on the CPU chip)—an environment where, with conventional design techniques, a system would be unreliable owing to excessive noise.

CENTRAL CONTROL. The CPU chip performs all processor functions except for floating-point–instruction execution and cache storage. This includes integer instruction processing, virtual memory management, cache control and interfacing, and managing the system and coprocessor interface buses. As part of this responsiblity, it takes charge of system timing. A 2X frequency-differential ECL-level synchronizing signal is sent to the CPU clock circuits. This on-chip clock generator not only provides the internal clock signals the CPU needs, but generates drive and latch clocks for the cache interfaces on the CPU and floating-point coprocessor, as well as signals to synchronize the coprocessor's on-chip clock generator.

The CPU's printed-circuit board was designed to permit this kind of control. Printed-circuit delay lines on the pc board allow the system to be optimized for different static RAM (SRAM) capabilities—either less-expensive, lower-performance devices or the newest high-speed parts. At 66 MHz, the system operates with off-the-shelf SRAMs whose access time is 12 nanoseconds. The SRAMs were determined to be a critical part in achieving the team's performance goals.

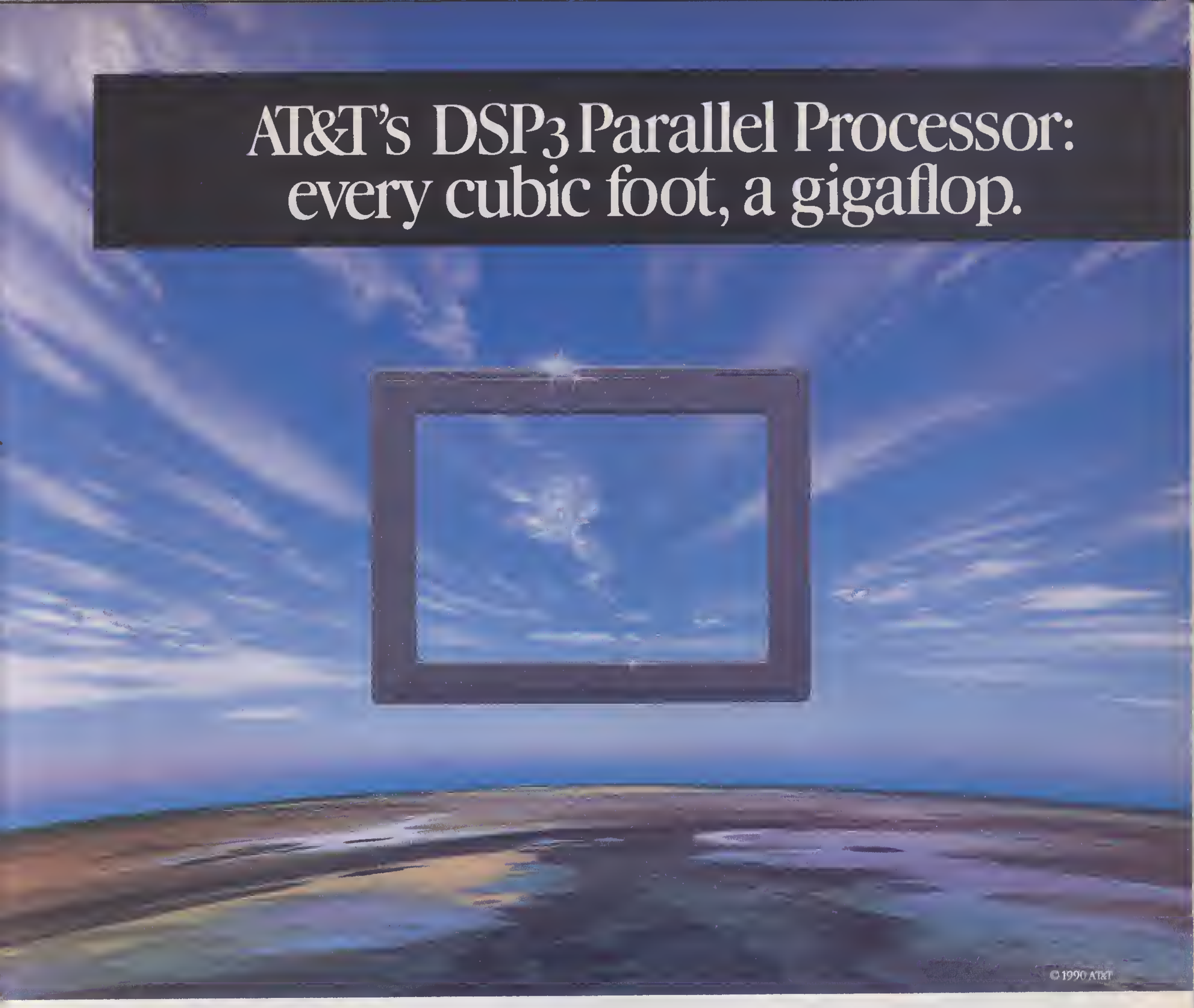
The CPU communicates with the instruction cache (I-cache) and data cache (D-cache) using separate address, data, and tag buses. The I-cache can range in size from 4K to 1M byte, while the D-cache ranges from 4K to 2M byte. For the I-cache, there is an 18-bit address bus; the data bus is 32 bits wide with a separate 20-bit tag bus. For the D-cache, there is an 18-bit address bus and a 64-bit data bus with a 22-bit tag bus. At 66 MHz, the I-cache data bus has a transfer rate of 264 megabytes per second, while the D-cache data bus's rate is 528 Mbytes/s. Again, to achieve this kind of performance required careful attention to bus layout on the pc board.

For executing integer arithmetic operations, the processor employs a five-stage pipeline. The key to fast operation is in optimally partitioning the operations that take place in each pipeline stage, increasing pipeline efficiency by minimizing stall conditions, and designing the pipeline clocking to allow high-frequency operation with external cache memory arrays. Also, the pipeline design takes advantage of compiler technology in which the compiler schedules events to avoid timing penalties. A branch-prediction algorithm is implemented on chip to eliminate many of the pipeline stalls that would normally result from executing conditional branch instructions. The clocking scheme and the pipeline partioning itself were designed to give the maximum amount of time to the off-chip I-cache and D-cache reads. All internal timing paths exceed the capabilities of current SRAMs.

The processor has separate internal buses and translation look-aside buffers (TLBs) to avoid timing penalties caused by simultaneous accesses to I- and D-caches. The buffers are used for translating virtual addresses to physical addresses. The TLBs are designed to minimize the miss rate (when information needed is not already in cache) and the associated timing penalties in a variety of ways. For example, the TLB provides four entries for variable-size blocks that can cover large memory areas—up to 16M bytes. These help reduce the miss rate by permanently mapping large areas of the operating system and graphics frame buffer. Further, the TLBs use a fully associative organization of 96 page translations each—a relatively powerful design for reducing TLB miss rates. Penalties resulting from TLB misses are reduced by implementing a set of shadow registers that automatically make backup copies of general registers.

The CPU and floating-point coprocessor were also designed to speed graphics operations. They support new instructions, among them clip-test integer multiply, inverse square roots, and pipeline I/O writes—all of which are important to high-performance graphics library routines. The high-speed execution of the standard integer and floating-point instruction set also assist in achieving graphics goals.

The coprocessor uses the same data and address buses as the CPU to communicate with the caches. With a 64-bit wide data bus,



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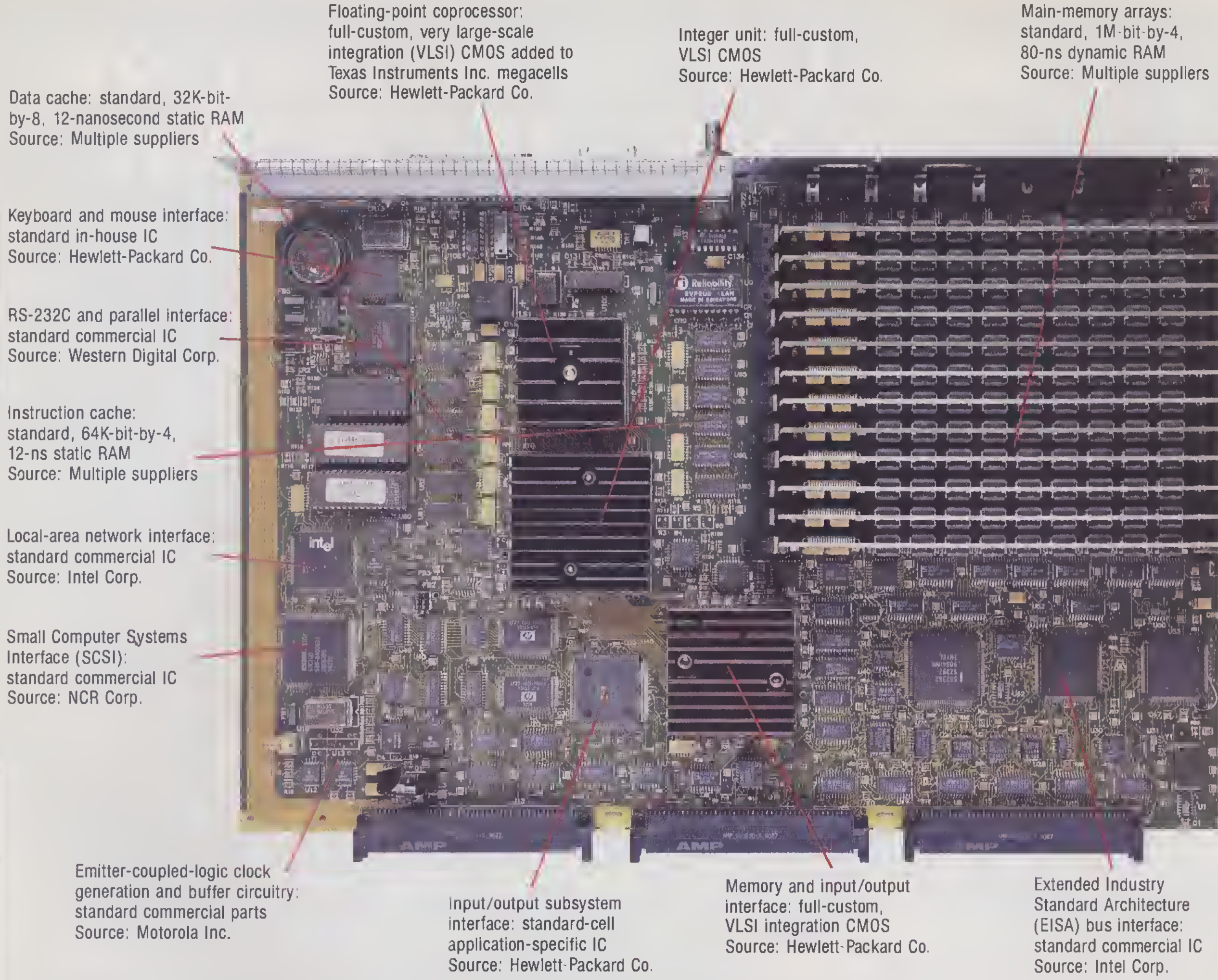

[2] The main printed-circuit board in the system mixes custom and off-the-shelf ICs.

it reads double-precision operands (or pairs of single-precision operands) from cache in a single clock cycle. Internally, the chip's data path and registers are all 64 bits wide. Portions of the integer unit's instruction-decode and pipeline-control circuitry have been duplicated on the coprocessor so that it can use instructions directly as they come from the I-cache.

Key to the exceptionally high floating-point performance are independent 64-bit floating-point functional units on the coprocessor chip. These include a multiply/divide/square-root unit and an add/subtract unit. These units are fed by a 32-by-64-bit register file, connected with eight separate 64-bit ports (five read and three write ports), to allow a high degree of independent parallel operation within the functional units. The PA-RISC instruction set has also been extended to include multiple-operation floating-point instructions. These combine a multiply operation with an independent add or subtract operation and complete the two in the same amount of time that a single operation would usually take—thereby doubling throughput in some situations.

CUSTOM VLSI HUB. The memory-I/O interface controller is a custom VLSI chip designed to meet three major performance objectives: optimize CPU servicing by main memory in the event of cache misses, perform memory arbitration among various I/O devices, and improve graphics performance. To fulfill these objectives, the chip is the hub of the system's three major data/address paths: the main-memory system bus, the CPU interface bus, and the System Connection to the I/O subsystems. The chip is produced in the same 1-μm process used to make the CPU chip, but is somewhat smaller at 185 000 transistors.

In addition to the memory-I/O controller, the main-memory system comprises an address buffer/controller, a data latch/multiplexer, and dynamic RAMs (DRAMs). The memory-I/O VLSI chip has error-detection and -correction (EDC) circuitry that corrects all single-bit errors and detects all multiple-bit errors.

The CPU communicates with the memory I/O controller through a private 66-MHz 32-bit bus that runs synchronously.

The memory-I/O controller was designed to work with 256K-by-4-, 1M-by-4-, or 4M-by-4-bit DRAMs. The timing and polarity of the control signals can be programmed at boot-up time. This allows different speeds of DRAMs and different loading (number of arrays) to be optimized. With 80-ns DRAMs, the memory system will fire first data back to the CPU 115 ns after the address has been received from the CPU. Subsequent data will be supplied at every 66-MHz clock edge.

The memory controller is optimized to service cache misses to the CPU. The cache line size is 32 bytes, and so the memory controller will provide the highest bandwidth when 32-byte blocks are accessed. The memory-I/O controller does support accesses as small as a single byte. High bandwidth can still be provided for smaller accesses because both reads and writes are buffered in 32-byte buffers.

Each bank of memory contains 36 DRAM chips (with a bus width of 128 bits of data and 16 bits of EDC). These banks are split into two memory array boards with 72-bit-wide buses. This means that the initial access to the bank returns four 32-bit words of data. TTL latching buffers are used to multiplex the 144 bits of data down to 72 bits that go into the memory controller. Simple deduction shows that to keep up with the 66-MHz, 32-bit bus, the TTL latches must be switched at 33 MHz and that the second set of data must be available from the memory bank at 16.5 MHz (60 ns). The fast-page-mode feature of the DRAMs is used to give this lower access time.

As noted, both the memory-I/O controller and the CPU have been designed to aid in graphics functions. While it is possible for

those systems to take over graphics performance completely, adding graphics subsystems via the System Connection can provide very high-quality graphics. For example, an external vector generator with dual buffers to prevent screen flicker can be implemented inexpensively with dedicated hardware. Such a graphics accelerator can produce over 1 million vectors per second, thus creating a 25 000-vector display in less than 1/30 of a second. This rate is more than acceptable for two-dimensional renderings and three-dimensional wireframes. For 3-D solids, the CPU can generate pixels at a rate of over 17 million pixels per second.

For even higher performance, graphics boards with geometry coprocessors and scan-conversion chips can be added. The System Connection, which has a peak bandwidth of 132 Mbytes/s, is fast enough to supply such a board with over 500 000 polygons per second. Further, it is also more than sufficient for handling X protocols and video displays.

I/O BUILT-IN. Besides graphics, the most common I/O functions required are communication, disk storage, and printing. While the interfaces needed to support these functions can be provided by separate add-in boards purchased by the user, this places a burden on communications and slows operation. Therefore it was decided to put the most common functions on a single board, which would not only keep system performance high, but actually lower the user's system cost.

Building the local-area network (LAN), Small Computer Systems Interface (SCSI), and parallel ports into the system allows them to directly access memory with very low latency. The logic that controls the interface between these functions and the system connection was implemented in a 15 000-gate CMOS ASIC.

EISA'S NICE. While it makes sense to incorporate commonly needed facilities on a dedicated workstation card, individual users may wish to add special functions to their systems. Since there is a wide variety of cards that work with 80X86-based personal computers, having an EISA bus in a system will allow the user to make use of them. Further, an EISA bus allows the user to add a 80X86-based board, thereby gaining the ability to run DOS applications along with the Unix applications that run on the RISC host.

To provide such capability, the team decided to create a converter that would let the system connection communicate with an EISA bus. Basically, the converter acts as a protocol translator.

There were two major points that had to be addressed in creating the converter: byte order and memory address space. The byte order problem occurs because the PA-RISC architecture stores the most significant byte of a word in the lowest numerical memory address, while the 80X86 architecture puts the least significant byte in that space.

(Continued on p. 68)

Efficient use

(Continued from p. 48)

porting of in-house–developed codes and interfaces to corporate systems as needed. The user interface will be enhanced through customization. The capacity to create icons, standard menus, selection options, and special application screens will eliminate computer-related frustrations frequently experienced by users.

The migration plan dictates that the electronic design workstation be an integral member of the overall environment. Capabilities such as Ethernet are fundamental elements. Concepts such as resource allocation, the sharing of expensive peripherals, and the ability to support a transitional environment and the migration of software applications are requirements. Local file servers and dedicated disk drives will support the requirements to store the application software and archive the CAD databases. Site software licenses will allow the interchangeable use of a variety of engineering applications on unrestricted workstation nodes across the network. Other issues such as unattended backups, security, and job accounting will be administrative facilities supported by a standard operating system.

Grumman's electronic design environment element of CIE will host a dedicated core of tools and capabilities that will accomplish the vast majority of electronic design tasks. The savings will be substantial and will come in varied forms: elimination of redundant systems, reduced maintenance expense, reduced training budgets, shortened learning curve, improved schedules, increased user proficiency, improved skill mix, superior quality, and so on.

THE FUTURE. The goal of the migration plan is to achieve a fully automated, data-driven environment where information is shared by all disciplines. However, to succeed at Grumman, it must be augmented by those principles inherent in what is being called concurrent engineering. Recent events in the Persian Gulf underscore the demanding degree of technology required to produce and to support today's weapons systems. To meet this challenge the proper design/development environment must be complemented by a change in the way engineers work—to concurrent engineering, or, as Grumman calls it, task-teaming.

In the past, the CAE/CAD/CAM process was somewhat serial in nature, one discipline handing off to the next as the task was finished. Today, a "shotgun" start is required to turn on all disciplines on a project simultaneously. The result of that start is task teaming, and the capability it provides is up-front design iteration by all disciplines involved in the realization of the product: thermal analysis, reliability, packaging, manufacturing, and so on, will all influence the product as the design process proceeds. Task teaming facilitates design changes when they are most manageable and easy to make. The result is product optimization—quality products manufactured with fewer errors in shorter time and at a lower cost.

A test case of CIE, now in progress, is the full electronic mockup of an avionics-system upgrade to an existing vehicle, the EA6B. The task is to develop aircraft wiring harnesses by using electronic design data and the vehicle's solid CAD model. Doing this will shorten product development time by about three months. It will also eliminate the need for an expensive hardware mockup to facilitate harness routing and speed up harness fabrication. Furthermore, fashioning such a hard mockup is fraught with an inordinate number of manual procedures, making the final product costly and subject to many errors.

The wiring harness solution will embody the full workstation environment and the task-teaming concept. The uniqueness of the process is the linking of electronic CAD design data with the structural CAD solid model. The engineers will be able to graphically route the harness and automatically determine cable diameters, wire lengths, clamp sizes, cable weights, applicable mounting hardware, quantities, and so on, and then transfer the appropriate data to the corporate parts list system.

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To probe further

Ergonomics and workplace design

The IEEE's position on emissions from workstations is given in *Biological Effects of Electric and Magnetic Fields from Video Display Terminals, An Entity Position Statement*, published on Aug. 13, 1990, by the United States Activities Board. The position paper not only explains the current state of research but also contains an excellent bibliography of recent guides and papers on scientific studies conducted in this area. It is available from the IEEE–United States Activities Office, 1828 L St., N.W., Suite 1202, Washington, D.C. 20036-5104; 202-785-0017.

With regard to extremely low-frequency effects, a scientific examination of the topic can be found in *Extremely Low Frequency Electromagnetic Fields: The Question of Cancer*, edited by B. W. Wilson et al. (Battelle Press, Columbus, Ohio, 1990). New developments in this area are highlighted in *VDT NEWS, The VDT Health and Safety Report*, a bimonthly newsletter published by Louis Slesin, Box 1799, Grand Central Station, New York, N.Y. 10163.

Advice on setting up a workstation environment is given in a report entitled *Improving VDT Work: Causes and Control of Health Concerns in VDT Use*, by Steven L. Sauter et al., Department of Preventive Medicine, University of Wisconsin, 1985. It discusses the major sources of eye and muscle strain and describes ergonomic factors in setting up a workplace. Its appendices contain checklists for chair and table requirements, as well as recommended exercises for relieving and preventing fatigue. It is published by the Report Store, 123 West 8th St., Suite 210, Lawrence, Kan. 66044, or telephone 913-842-7348.

Considerations for area lighting are reviewed in *Solving the Puzzle of VDT Viewing Problems*, a 1987 publication of the National Lighting Bureau, Washington, D.C. Theoretical as well as practical information and standards for ergonomic design are provided in *Video Displays, Work, and Vision* by the National Research Council's Panel on the Impact of Video Viewing on Vision and Workers, National Academy Press, Washington, D.C., 1983.

Information from several of the above sources formed the basis for workplace layouts and physical dimensions presented in this guide.

Technical information on workstations

An excellent book on the architectures of modern computer systems, including workstations, is *Computational Structures*, by S. Ward and R. Halstead Jr. (MIT Press and McGraw-Hill Book Co., 1990). The text looks at computers from a system level, explaining the influence of software on hardware structures; it covers all major modern architectures, including reduced-instruction-set computers, and architectural subsystems.

Both *IEEE Computer* and *IEEE Micro* magazines regularly feature articles on system architectures, components, and implementation methods.

The Computer Society Conference has become a focal point for discussions of the newest workstation architectures. At this year's Compcon in San Francisco, Feb. 25–March 1, attendees heard a number of papers on the Hewlett-Packard workstation design discussed in the article that starts on p. 58. For information on future conferences and on obtaining copies of the proceedings, contact the IEEE Computer Society, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036-1903, or call 202-371-1013.

The ACM/IEEE Design Automation Conference, while focusing on software, also shows attendees the hardware they will need for electrical engineering design. This year, the conference will be held June 16–20 in San Francisco. For information, write or call MP Associates Inc., 7490 Clubhouse Rd., Suite 102, Boulder, Colo. 80301; 303-530-4333. ◆

Acknowledgments

In preparing this special guide to engineering workstations, *IEEE Spectrum* called upon many experts. We are especially indebted to the following individuals for their advice and guidance, although their identification with the guide should not be construed as their endorsement of any of the opinions or products covered in its pages, nor of the accuracy of its statements.

The advisers for this guide were: Brush Bradley, marketing manager for Digital Equipment Corp.'s Engineering Systems Group, Marlboro, Mass.; Gene A. Grindstaff, Intergraph Corp., Huntsville, Ala.; Bill Meyer, platform engineering manager, Mentor Graphics Corp., Beaverton, Ore.; Eric E. Schmidt, vice president of Sun Microsystems Inc.'s General Systems Group, Mountain View, Calif.; and Carl Zeitler, hardware architecture manager, IBM Corp., Austin, Texas.

In the area of ergonomic engineering, special assistance in the review of the material was provided by Thomas S. Tenforde of Battelle Corp.'s Pacific Northwest Laboratories in Richland, Wash.

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EDITORIAL

WORKSTATION SELECTION

ICs' impact

(Continued from p. 65)

Therefore, at the interface between the two worlds, the data lines are wired to swap bytes into the right order.

However, if control data needs to be written into the registers of EISA cards from the RISC side of the system, the interface would erroneously swap the bytes. To correct for this situation, the RISC CPU swaps the order of all multibyte control words before sending them to the EISA registers.

For the two halves of the system to work cooperatively, the memory address spaces of the two buses have to converge. From the RISC side, all of EISA's 64K-byte I/O address space is mapped into part of the PA-RISC address space. A fixed portion of the EISA memory space is also mapped into the PA-RISC space.

EISA cards, though, may need access to the RISC main memory so that they can download data using DMA to a destination buffer. Such a scheme means that data need not be copied to memory twice, which would effectively decrease bus throughput. To provide this kind of access, addresses generated by an EISA direct-memory-access card that fall into a specified range of the EISA memory address space actually address a SRAM on the bus converter. This RAM's output replaces the upper 20 bits of the EISA address memory with a page number in the RISC system's main memory.

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Mark Forsyth, a project manager at HP's Engineering Systems Laboratory, Fort Collins, has participated in the design of four 32-bit VLSI processors since joining HP. His recent responsibilities include managing the design of the CPU and cache memories. He received a BSEE degree from the University of Minnesota in 1978.

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Larry J. Thayer is a hardware design engineer in the HP Graphics Technology Division, in Fort Collins. He has specialized in the design of graphics subsystems and processors. Most recently, he has worked on the development of custom VLSI components. He received his BSEE and MSEE degrees from Ohio State University. ◆

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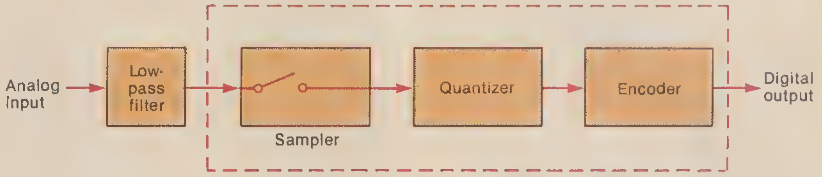
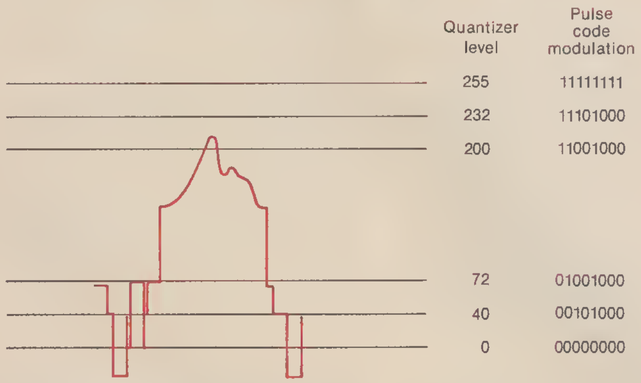
Analog in, digital out

A basic method for converting the analog signal outputs from a high-definition television camera into digital signals is pulse code modulation (PCM). An analog-to-digital converter [see illustration] is preceded by a low-pass filter that confines the signal to a limited spectrum to prevent spurious components from appearing in the reconverted analog output.

The converter samples the analog input, measuring its amplitude at regular intervals of time. The sampled amplitudes are then matched in the quantizer against 256 levels of amplitude so that each of these levels can be represented by an 8-bit word. (Eight-bit words are most commonly used in television, and since each bit can be either a 1 or a 0, there are 2^8 or 256 different ways that the 1s and 0s can be arranged.) The error in amplitude is about 0.4 percent after quantization, which is equivalent to 48 decibels below the maximum signal level.

The process of matching each sampled amplitude with its unique digital word is the job of the encoder. It scans the list of words and picks out the one that matches the sampled amplitude at any time. The encoder then outputs the series of digital words in the same sequence as the one in which the analog signal was sampled. The list of digital words corresponding to the sampled amplitudes is known as a code.





The accompanying waveform is shown with several quantized amplitude levels based on the PCM scheme.

In the television receiver, the reverse occurs. A digital-to-analog converter contains a decoder that outputs an analog signal corresponding to the original one produced by the camera. —*R.J.*

This description is based on material in the book "HDTV—Advanced Television for the 1990s" *by K. Blair Benson and Donald G. Fink [see To probe further].*

(Continued from p. 30)

pect ratio. To fit the digital HDTV signal into a 6-MHz channel, it uses an algorithm based on transform coding. The particular type of transform used is called a discrete cosine transform (DCT). It transforms an 8-by-8 block of pixel intensities into an 8-by-8 block of frequency transform coefficients. The transform is applied in turn to new blocks until the entire image has been transformed. At the decoder in the receiver, the inverse transformation is applied to recover the original image.

The property of the DCT that makes it possible to compress the image is this: for typical images, just a few transform coefficients suffice to compact much of the signal energy. For example, one transform coefficient in an 8-by-8 block represents the dc energy of the entire block.

With a process called normalization, the number of transform coefficients that must be used is reduced. First, an algorithm is used to assign a variable number of bits to those coefficients, and then Huffman statistical coding is used to assign relatively short code words to events with the highest probability of occurrence.

In yet another step in the DigiCipher system, the signal is compressed yet again by first predicting how the next frame will appear and then sending the difference between the prediction and the actual image. The previous frame is often a reasonable predictor. This DPCM procedure works best with pictures containing only little motion.

Motion compensation is applied by determining what has moved since the previous frame. Once this information is known to the decoder in the receiver, a portion of the previous frame can be shifted or displaced in order to obtain a more accurate prediction of the next frame that has yet to be transmitted. The decoder reproduces the same prediction as the encoder at the transmitter and then determines the difference between the prediction and the actual image.

A chrominance preprocessor reduces the resolution of chrominance information relative to luminance resolution. First it separates the signal into luminance and chrominance components. The luminance signal maintains full resolution, but a prefilter is used on the chrominance components to average pixels in groups of four horizontally and groups of two vertically. The chrominance components are then multiplexed with the luminance component. At the decoder in the receiver, the components are again separated and reproduced.

The DigiCipher system uses a sampling frequency of 51.80 MHz for the chrominance and luminance signals. A forward error-correcting encoder adds error correction bits to the 16 quadrature-amplitude-modulated (16-QAM) data stream (which includes four audio signals as well as the video signals).

ZENITH-AT&T SYSTEM. The Zenith-AT&T Digital-Compatible HDTV System (DSC-HDTV) is an extension of Zenith's previous analog-digital system. DSC-HDTV is said to reject NTSC cochannel interference into the DSC-HDTV channel, providing an HDTV service area equal to that of an NTSC broadcast station while radiating at least 12 decibels less power. The previous system's simulcast feature in a 6-MHz band, its NTSC-like transmission signal timing, and the low power are all retained.

DSC-HDTV uses progressively scanned video signals of 787.5 lines per frame and 59.94 frames per second. That corresponds to 1575 horizontal picture lines 30 times per second to create a completely new picture with a 16:9 aspect ratio 60 times a second. Square pixels allow easy graphical interfacing with computer workstations as well as production of special effects

A video compression algorithm developed by AT&T Bell Laboratories enables 34 MHz of picture information to be squeezed into a single 6-MHz channel. The algorithm is embodied in high-speed digital signal processors developed by AT&T Microelectronics.

Using only the luminance frames, motion from frame to frame is estimated by a hierarchical block-matching motion estimator. It produces motion vectors, which are compressed and sent to the output buffer for transmission. Using predictive encoding, the small differences between the new image data and the motion-compensated predicted image data are encoded through adaptive transform coding.

(Continued on p 73)

A critique of purely digital HDTV

Less than two years ago, the nearly universal view of the U.S. television industry was that high-definition television (HDTV) must be compatible with today's National Television System Committee (NTSC) broadcasting system. Everyone recalled the introduction of color in 1953, when, to preserve the utility of the 10 million sets already in existence, the color signal was made directly viewable on monochrome receivers. A second view, just as strongly held, was that signal compression systems of any kind would downgrade quality too much to be acceptable.

Both views were wrong. The problem addressed by compatibility is service to existing receivers. Simulcasting, used later in Britain and France when color was introduced there, has proved a better solution and has now been accepted, albeit reluctantly, by the U.S. industry. As for compression, many effective systems have been demonstrated, including one at the Bell-Northern Research Laboratory in Montreal about 10 years ago, which enabled full NTSC quality at only 6 megabits per second.

Today's situation is remarkably similar. Important decisions are being made without adequate thought. Not only has there been a complete turnabout on the feasibility of compression, but a stampede is developing in favor of digital terrestrial broadcasting, which has yet to be shown to be practical in the face of analog channel impairments such as ghosts, noise, and interference, not to mention the effect of rabbit-ear antennas.

Of course, digital over-the-air broadcasting could prove feasible in the future. But certainly no proof of this as yet exists, and apparently little or no work is now going on in this field. But if efficient over-the-air digital transmission proves impractical, and all the U.S. HDTV proposals are all-digital, then the likely winner of the FCC bake-out will be Japan Broadcasting Corp.'s multiple sub-Nyquist encoding (MUSE), which would hardly be to the advantage of the United States.

SOURCE AND CHANNEL CODING. Compression systems fall into the category of source coding systems, while modulation methods used for transmission are channel coding systems. All the HDTV systems so far proposed to the Federal Communications Commission (FCC), without exception, use digital compression methods. All-digital systems, which use both digital source coding and digital channel coding, are being advertised as more effective compression schemes. True, there is a connection between channel and source coding; but it is not true that digital transmission invariably means better compression.

All the HDTV compression systems so far proposed are based on subband coding or the discrete Fourier transform, a special case of subband coding, in which much of the data to be transmitted consists of adaptively selected coefficients, or subband samples, which are, in effect, image samples. Such data gains nothing by being transmitted in digital form. At least as effective an overall system can be designed around hybrid schemes, in which digital transmission is used for audio and decoding data, and analog transmission for the image samples. Just as good source coding is possible and higher channel coding efficiency is achieved.

Because very poor spectrum efficiency is attained in much of the viewing area by the digital transmission systems so far proposed, extremely complex source coding is required, which increases the complexity of receiver signal processing. Hybrid systems, with their much higher spectrum efficiency, can use simpler source coding algorithms with correspondingly simpler receiver processing.

OTHER DIGITAL TRANSMISSION MYTHS. Several other myths are connected with digital transmission, notably:

- *Digital modulation is the most efficient method of transmission.* In reality, analog amplitude modulation is the most efficient method of transmission in an analog channel, in terms of information delivered for a given channel capacity (which depends on both bandwidth and signal-to-noise ratio).

Digital transmission's invariable loss of transmission capacity can, in theory, be made vanishingly small. But, in practice, digital transmission schemes rarely achieve even half the theoretical channel capacity, and then only when the modulation method is designed for a particular signal-to-noise ratio at the receiver. But in terrestrial broadcasting, the signal varies widely as a function of range. Therefore, for systems that deliver a fixed number of bits per second throughout the receiving area, transmission efficiency is high only in the fringe area.

- *Digital systems have better interference performance than analog systems.* Digital systems achieve their legendary freedom from interference by giving up additional channel capacity. Nonetheless, it has never been proved—and probably is not true—in a given channel at a given (significantly smaller) transmission rate, that digital systems have better interference performance than analog systems.
- *Digital transmission is more free from noise than analog transmission.* When a signal is digitized in order to prevent the accumulation of noise in a long series of amplifiers, channel noise is replaced by quantization noise, which is always larger than the channel noise to be overcome. Signal quantization in such cases is a matter of convenience, and not a means of improving transmission efficiency.
- *Ghosts are automatically removed by digital transmission.* Ghosts can be thought of as a kind of self-generated interference, and the same considerations apply as in the case of interference from other television stations. Ghosts are not automatically removed by digital transmission, but must first be removed in order to permit digital transmission at useful rates.

Overall, in fact, if ghosts, noise, and interference in the over-the-air channel could be cleaned up enough to achieve efficient digital transmission, the quality of NTSC signals transmitted in such channels would also be greatly improved—so much so that the further perceived improvement due to the higher resolution of HDTV would be quite small.

- *Digital transmission simplifies interoperability with nonbroadcast applications.* The difficulty in transcoding to other signal formats is primarily a question of relative resolution, scan rates, and aspect ratio, and not whether the signal is analog or digital. In any event, all proposed HDTV encoders and decoders are entirely digital; it is only the terrestrial transmission format that might be hybrid. Conversion from it directly to nonbroadcast formats will occur only rarely. Conversion will be done to computer workstation format, for example, primarily from the production or international exchange formats.

SPECTRUM EFFICIENCY. Spectrum assigned to television cannot be used for any other purpose. A corollary is that the highest possible image quality and the maximum number of channels should be available to each viewer within a given overall spectrum allocation.

In these terms, simple-minded digital systems that deliver the same number of bits per second to all receivers in the service area necessarily waste channel capacity in the central cities, precisely where a spectrum shortage is developing because of the rapid growth of cellular telephones and other mobile services.

One way to deal with this problem is to use hybrid analog-digital transmission, in which image quality improves with signal-to-noise ratio, just as it does in purely analog systems. Possibly this could also be done with a sophisticated digital channel coding method, but no such method has yet been proposed to the FCC.

To put this in the most dramatic way possible, an alternative to delivering, say, 20 megabits per second in 6 megahertz would be to use a hybrid analog-digital format delivering 10 Mb/s plus 10 megasamples per second in 3 MHz. Most viewers in the service area would receive more information with the hybrid system and, with appropriate source coding, would get better pictures; yet only half the bandwidth would be used.

In spite of what may appear from the foregoing, I am very enthusiastic about digital HDTV systems—certainly for compression and possibly for transmission. The latter is probably the method of choice for clean channels with well-defined signal-to-noise ratios, such as direct-broadcast satellites and optical fiber.

Nevertheless, if we are serious about using digital transmission in the over-the-air channel, it will first be necessary to demonstrate conclusively that it can be made to work with adequate reliability and spectrum efficiency. —*William F. Schreiber*

The opinions expressed here are those of the author alone.

William F. Schreiber (F), emeritus professor of electrical engineering, Massachusetts Institute of Technology, Cambridge, was the designer, along with a number of colleagues and students, of MIT's hybrid HDTV system, now withdrawn and replaced by an all-digital system.

The displaced frame difference is encoded using a spatial transform, and the resulting coefficients are quantized. Luminance and the two chrominance difference pixels are encoded separately. The encoded video is packed into a special format before transmission, which maximizes immunity to transmission errors by masking the loss of data in the receiver decoder. Thus, the duration and extent of picture degradation due to any one error or group of errors is limited.

With the video encoder generating about 17 megabits per second, all data bytes are protected by the Reed-Solomon codes except the sync interval bytes—because sync detection must take place before error correction—and spare data bytes, which are not currently assigned.

Output from the video encoder is fed to a data formatter and error control system where the video bit stream is combined with digital audio, ancillary data, and Reed-Solomon error control bytes. After the resulting data stream goes to a prefilter where preprocessing takes place, a pilot signal is added to the transmission signal to aid carrier recovery at the receiver, and encoded synchronization signals are also added.

The DSC-HDTV system uses pulse amplitude modulation with vestigial sidebands. The number of possible amplitudes is limited to four. Compared to continuous amplitude modulation, this provides immunity to thermal noise and other impairments.

PHILIPS-SARNOFF SYSTEM. Advanced Digital Television (ADTV) is the name of the entry from the Advanced Television Research Consortium. The system uses 1050-line interlaced scanning at a 59.94 field rate with a 16:9 aspect ratio.

The video compression technique used, called MPEG^{++}, upgrades the compression approach to HDTV performance level of the Moving Pictures Expert Group (MPEG)—a committee within the International Standards Organization—to provide high-quality HDTV pictures at 20 Mb/s. MPEG is a collection of compression methods, including motion estimation, motion-compensated predictive coding, adaptive DCT quantization, and variable-length coding-decoding. The compression technique also incorporates a video data prioritization layer that allows the most important video data to be transmitted with the greatest reliability.

Another feature, Prioritized Data Transport layer, is a fast-packet cell transport format in which information bits are carried in cells consisting of fixed-size data, header, and trailer. This format permits relative ease in switching and routing—even at high speeds. A well-known example of such a format is the asynchronous transfer mode protocol in the broadband integrated-services digital network. Cell relay provides rugged logical synchronization that is essential for reliable delivery of variable-length coded compressed video in the presence of transmission errors.

ADTV uses quadrature amplitude modulation with spectral-shaping techniques, together with Reed-Solomon forward error correction channel coding, to minimize interference from and to any co-channel NTSC signals. The correction codes are applied to the data bytes before the carrier-modulation stage. Depending on the priority, different codes are applied to the data. In addition, data interleaving is performed as part of the channel-coding operations to ensure that bursts of channel bit errors can be treated as uncorrelated random bit errors, which can often be corrected by the Reed-Solomon codes.

ADTV provides for up to four digital CD-quality-sound audio channels that nominally make up two stereo pairs. Audio compression closely follows Masking-Pattern-Adapted Universal Subband Integrated Coding and Multiplexing (Musicam), the industry standard for broadcast digital audio.

> Important decisions are being made without adequate thought

Although submitted as a 1050-line system, ADTV is designed to provide flexible support of a wide range of services and future media formats.

AMERICAN TELEVISION ALLIANCE SYSTEM. The ATVA-Progressive System from MIT on behalf of the American Television Alliance provides a video signal with 720 by 1280 pixels, a 16:9 aspect ratio, progressively scanned at 59.94 frames per second.

The encoding part of the system consists of conversion of red, green, and blue components into Y (luminance) and U, V (chrominance) components. It also uses source adaptive encoding, motion estimation and compensation, transform-subband analysis of motion-compensated residuals, adaptive selection of high-energy transform-subband coefficients, quantization of the selected coefficients, entropy coding of the quantized coefficients, and data multiplexing-modulation. The audio signals are also digitally encoded.

For motion compensation, a prediction is made for the current frame to be encoded from the previously encoded frame and the motion vectors. The difference between the current frame to be encoded and the prediction (the motion-compensated residual) is then computed for Y, U, and V. When the motion-compensated residual has sufficiently large energy relative to the image frame, motion compensation is disabled, and the image frame itself is encoded. This is the case with scene changes, for example.

Each of the Y, U, and V components is analyzed by a transform-subband analysis filter that divides the residual into 8-by-8 bands. To exploit the variation in sensitivity of the human visual system, the transform-subband coefficients are weighted according to the frequency band and luminance-chrominance components. The weighted coefficients are selected on the basis of their energy; those with the highest energy are selected until the required number of bits to encode reaches the limit available (0.24956 Mb). The video bit rate required is this number times 60 frames per second, or 14.99 Mb/s.

The location and amplitude of each chosen transform-subband coefficient are encoded jointly using a Huffman encoding method.

The digital video information is multiplexed together with four digital audio channels, an auxiliary 0.126-Mb/s data stream, and 0.126-Mb/s access control to form the composite 19.143-Mb/s digital stream. The auxiliary data stream is made available for transmission of closed captions or other digital data. Sync bits are inserted into the transmitted bit stream to mark the frame boundaries.

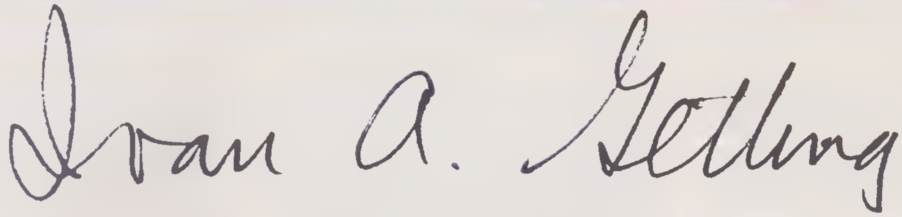
Reed-Solomon coding is used to correct transmission errors caused by noise and interference. The system threshold is 19-dB carrier-to-noise ratio. At that threshold, there is one undetected error event per day.

For digital transmission, a single carrier with double-sideband, suppressed-carrier quadrature modulation is used. The quadrature signal is generated at a sampling frequency of 4.86 MHz. Spectral shaping filters in the transmitter limit the signal to a 6-MHz double-sided bandwidth. A digital filter is used for spectral shaping.

TO PROBE FURTHER. The technical discussion in this article is based in part on two books. The first, *HDTV—Advanced Television for the 1990s*, by K. Blair Benson and Donald G. Fink (Intertext Publications, McGraw-Hill, New York, 1991), provides excellent background on advanced television systems of all kinds, with limited material on digital HDTV. The second, *Digital Pictures—Representation and Compression*, by Arun N. Netravali and Barry G. Haskell (Plenum Press, New York, 1988), gives detailed technical information on the various basic compression techniques.

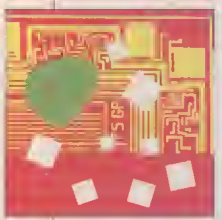
A third book, *Signal Processing of HDTV, II*, edited by L. Chiariglione (Elsevier, Amsterdam, the Netherlands, 1990), contains papers from the Third International Workshop on HDTV held in Turin, Italy, Aug. 30–Sept. 1, 1989. Many of the papers address motion estimation, preprocessing, and HDTV transmission on digital channels.

A new report on video compression techniques and their commercial applications is available from IGI Consulting Inc., 214 Harvard Ave., Suite 200, Boston, Mass. 02134; 617-738-8088. ◆



Ivan A. Getting

The founding president of the Aerospace Corp. was the force behind the Navstar global positioning system of satellites



Part of the coalition forces in the Persian Gulf might have been lost in the desert were it not for a vision that Ivan A. Getting had in 1960 and pursued relentlessly for the past 30 years. At the very least, the military might not have been able to locate their precise positions or know exact coordinates as easily, a crucial advantage in commanding and controlling forces in the desert and on the sea, and in deploying surgical-strike weapons.

Getting's vision is Navstar, the global positioning system of satellites. It dates to the 1940s, when Getting was a researcher working on radar weapons control systems at the Radiation Laboratory at the Massachusetts Institute of Technology (MIT) in Cambridge. His colleagues in a nearby lab were developing the navigation system used today by ships and planes, Loran. Using land-based transmitters to send signals to a receiver on the missile, Loran compares the arrival times of the different signals to calculate its position.

In the 1950s, as head of research and engineering at Raytheon Corp., Waltham, Mass., Getting led a project to develop a mobile ballistic missile guidance system called Mosaic, which was to work like the Loran system. But Getting envisioned another concept. Though the railroad mobile version of the intercontinental ballistic missile was canceled, he realized that if a similar system were used, one that based the transmitters on satellites, and if enough satellites were lofted so that four were always in sight, it would be possible to pinpoint locations in three dimensions anywhere on earth. This theory led to Navstar.

In 1960 Getting was asked by the U.S. Air Force to create a nonprofit military systems development organization, the Aerospace Corp. in El Segundo, Calif. During the hectic early days of building the new company, he assigned a planning group to look at the feasibility of his idea to navigate globally by satellites. Though as president of the Aerospace Corp., he took on many complex projects—planning new ballistic missile systems, overseeing space launch systems, and developing high-powered chemical lasers—global satellite navigation remained his constant passion.

FINDING FUNDS. It was clear from the start that Navstar would require at least 18 satellites for worldwide coverage and would cost billions of dollars.

His biggest concern, he recalled, "was to get the damn thing funded." He became an evangelist for Navstar, promoting it at every opportunity to the presidential science advisor and to the heads of the various armed forces. "I was selling everywhere, promoting, promoting," Getting said.

"Ivan is relentless in pursuing an objective," Sam Tennant, the current Aerospace Corp. president, told *Spectrum*. "Navstar was not a program that came easily. In the early days, there were few believers."

> 'Ivan is relentless in pursuing an objective.'

But eventually people started buying into Getting's project, although with some reluctance. The Air Force consented to fund a study. The R&D board of the Department of Defense agreed to fund a technology demonstration. And finally, the Department of Defense approved funding of the development and deployment of a complete Navstar system, costing some US $10 billion.

The first Navstar satellite was launched in 1978; by 1985 enough satellites were in orbit for Navstar to be used, at least in two dimensions, in most areas of the world. Complete worldwide coverage was expected to be available by 1987, but the launch schedule was set back by the Challenger disaster. Its scheduled completion date, with 18 satellites sending out signals, is now set for 1993.

Navstar now fully covers the Persian Gulf area, and coalition forces carry thousands of receivers that can calculate positions within accuracies of less than about 9 meters (30 feet).

Today Getting is theoretically retired, but he shows little sign of slowing down and talks warmly about the experiences of his long career. When he is not on the road, advising companies and the Department of Defense, he spends much of his time in a crowded office in his Brentwood Park home in Los Angeles, a stone's throw from Hollywood stars. There, he is surrounded by stacks of documents demanding attention (his filing system has deteriorated since he gave up corporate life and the personal secretary that went with it). In his free moments, he retreats to a tiny backyard greenhouse, where he raises orchids.

PATRIOT PREDECESSOR. Navstar was not the only military technology used in the Persian Gulf conflict associated with Getting's research efforts. The Patriot missile—the so-called Scudbuster—uses radar and computers to home in on attacking missiles. It is a sophisticated version of a radar-based automatic antiaircraft system Getting worked on during World War II—the SCR-584.

This was the first system to use radar and computers to calculate missile paths. It was a hands-on project: Getting and his team built a demonstration system in 1941, working in an old World War I hangar at MIT, in the middle of the winter, with no heat. By 1944 some 300 SCR-584s were placed around London, and they logged a success rate of 95 percent in shooting down Germany's V-1 cruise missiles.

The SCR-584 also tracked the V-2 ballistic missile (a forerunner of the Scud) and traced its path backward—to its launch site—as well as forward; launch site coordinates could be quickly radioed to fighter-bombers and swiftly attacked. When the Patriot was designed, this feature was deleted from the system specifications, Getting said, because of concern that such a capability would cause the Patriot to be classified as an offensive, rather than defensive, weapon.

For his work on the SCR-584, Getting received the Medal for Merit from President Harry Truman in 1948, one of 15 scientists so recognized that year.

CAREER CHOICE. While Getting's parents did not have a scientific bent—his father was involved in Slovakian politics and publishing—Getting seems to have been born with an interest in technology.

Tekla S. Perry Senior Editor

Ron Mesaros (photo)

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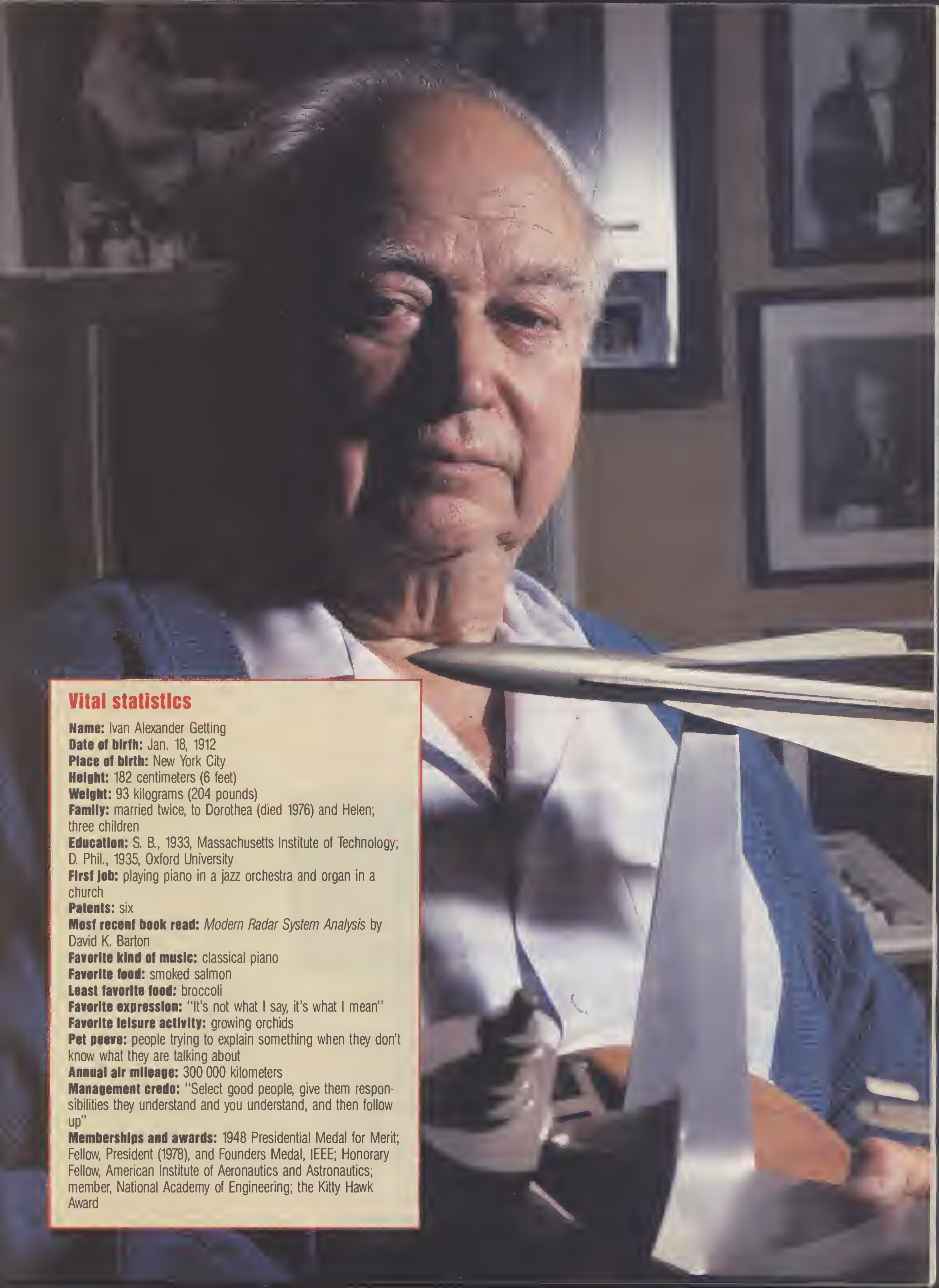

Vital statistics

Name: Ivan Alexander Getting
Date of birth: Jan. 18, 1912
Place of birth: New York City
Height: 182 centimeters (6 feet)
Weight: 93 kilograms (204 pounds)
Family: married twice, to Dorothea (died 1976) and Helen; three children
Education: S. B., 1933, Massachusetts Institute of Technology; D. Phil., 1935, Oxford University
First job: playing piano in a jazz orchestra and organ in a church
Patents: six
Most recent book read: *Modern Radar System Analysis* by David K. Barton
Favorite kind of music: classical piano
Favorite food: smoked salmon
Least favorite food: broccoli
Favorite expression: "It's not what I say, it's what I mean"
Favorite leisure activity: growing orchids
Pet peeve: people trying to explain something when they don't know what they are talking about
Annual air mileage: 300 000 kilometers
Management credo: "Select good people, give them responsibilities they understand and you understand, and then follow up"
Memberships and awards: 1948 Presidential Medal for Merit; Fellow, President (1978), and Founders Medal, IEEE; Honorary Fellow, American Institute of Aeronautics and Astronautics; member, National Academy of Engineering; the Kitty Hawk Award

But the choice of military engineering seemed less ordained. Getting did not spend his childhood building model aircraft or in fantasizing about building real planes and tanks. Rather, he fell into a military career almost in spite of himself.

As a child in Perth Amboy, N.J., he received a hand-me-down Meccano set—a toy that competed with Erector sets—consisting of plates, gears, axles, and other metal parts. With the set he figured out how a car's differential worked. He went on to study physics at MIT, winning a scholarship in a contest to find Edison's successor. Graduating in 1933, the depths of the Depression, Getting had no hope of finding a job in his field, so he applied for a Rhodes scholarship and studied astrophysics at Oxford University in England. This was followed by studying nuclear physics at Harvard University in Cambridge, Mass., where he developed the first high-speed flip-flop.

Then, he says, "I got trapped by the war." The Radiation Laboratory was established at MIT to work on radar as part of the war effort, and a Harvard scholar in the office next to Getting's was tapped to head the project. He recruited Getting, reasoning that the circuitry Getting had been developing to examine cosmic rays could be applied to radar.

When the war ended in 1945, the Rad Lab was disbanded. Getting chose to stay at MIT as an associate professor of electrical engineering, intending to do research in nuclear power, which he considered a vital field. "We need power for everything we do, from lights to producing fertilizer," he explained. "This was an opportunity to make what was considered an infinite source of power."

But the doors to nuclear power research were locked because of concerns over security—only people who had been in nuclear research during the war could get in. So Getting turned his research to electron accelerators, building a 350-megaelectronvolt synchrotron. Lack of a synchrotron industry, however, forced him to focus his consulting on military systems and radar. After war broke out in Korea in 1950, the Air Force wooed him to its staff in the position of assistant for development planning. His career path in military systems was set.

GREATEST BLOOPERS. While Getting's successes have been formidable, he is the first to admit that he has made his share of mistakes. Early in his career, these errors taught him to pay attention to even the smallest details of an engineering effort.

In 1939 at Harvard, Getting worked feverishly to repeat a German experiment and be the first in the United States to demonstrate fission. Using an old bell jar to create a cloud chamber within which to observe fission reactions, he took thousands of pictures—but none showed fission particles. After Columbia University in New York City announced that it had demonstrated fission, Getting discovered that his bell jar was very old and had been made of boron glass, which absorbed the slow neutrons needed to produce fission of uranium.

The following year, in an attempt to test radar tracking at the Rad Lab, Getting inflated a rubber balloon with hydrogen. Over the balloon he draped reflective aluminum material attached to raw silk. But the balloon rubbed against the silk in the wind, creating a static charge, then a spark, then an explosion that singed Getting's hair and eyebrows.

When Raytheon in 1950 had a problem with tubes that met their specification tests in the factory but failed in the Navy acceptance tests of the altimeters, production stopped while the problem was investigated. It turned out that a technician making final adjustments was using an unmatched homemade radio-frequency coaxial cable instead of a standard production cable. It cost the company $300 000 to find the error, and throughout his tenure at Raytheon, Getting kept that cable in his desk as a reminder of what can happen when a detail is missed.

This learned obsession with details, which Getting tried to impress on every employee, served the Aerospace Corp. well when it took on the responsibilities of manned space launches. Aerospace oversaw all the launches in the Mercury and Gemini programs, and the company impressed on every contractor the importance of tender loving care—paying attention to every detail. "We never lost a single astronaut," Getting said. When TLC was reduced, the inevitable human error did slip through.

ENGINEERING ENVIRONMENTS. After his first few years at the Rad Lab, Getting made his first move from engineering into management. But once the lab folded in 1945, he turned down several offers of engineering management jobs to return to university teaching and research. However, he was persuaded in 1950 to move to the Air Force staff, and he never went back to hands-on engineering.

> 'I didn't want to be one of a thousand. I wanted individuality.'

As a manager, Getting believed in treating employees with respect and care, even though this was counter to many corporate philosophies at the time. When he joined Raytheon as vice president, engineering and research, in 1951, the company, like many of its New England competitors, housed its engineers in old brick textile factories, crowding them into large open areas.

But Getting knew that engineering environments could be different, and that AT&T's Bell Laboratories, Murray Hill, N.J., had made a start in effecting such a change by building attractive, landscaped, pleasant facilities for its engineers, giving each a private office. He thought Bell had the right idea and launched a building program at Raytheon on Route 128 outside Boston.

"I had been a working engineer myself," Getting told *Spectrum*. "I didn't want to be one of a thousand. I wanted individuality. Scientists and engineers, if they are any good, want individuality; they want an opportunity to get together with other engineers, but they don't want to be herded like sheep. And the cost of adequate office space is the smallest part of the total cost of operating a high-tech company."

Besides prime facilities, Getting advocates giving engineers a chance to get credit for what they accomplish, and as much public recognition as possible. This is not always easy for military contractors, when engineers are barred for security reasons from even mentioning their work to their families.

Max Weiss, a former director of Aerospace's R&D laboratories and now vice president of Northrop Corp., Los Angeles, told *Spectrum* that Getting seemed able to provide this positive motivation intuitively. "He would take a younger man, put his arm around him, and encourage him," Weiss said. "He gave me a lot of self-confidence and encouraged my initiative. Today we would call it empowerment."

Since his retirement in 1977, Getting seems barely to have slowed down. He served as IEEE President in 1978, is currently a member of the board of directors of several companies, and is on the Air Force Scientific Advisory Board as well as on the Navy Studies Board of the National Research Council—responsibilities that require several trips a month from his home in Los Angeles to Washington, D.C.

Northrop vice president Weiss told *Spectrum* that Getting is invaluable on such boards and committees because he asks penetrating questions in a disarmingly naive way. "He'll say: 'Forgive me, I'm an old man, you're smarter than I am, you'll have to explain this to me,' " according to Weiss. Then he will zero in with a pointed question.

All these activities leave Getting little time for raising orchids, a hobby he began in the 1930s, or playing the piano. (He occasionally accompanies TRW founder Simon Ramo, a violinist.)

And, since Navstar is not quite completed yet, and plans for future generations are still being made, Getting, now age 79, is still evangelizing.

TO PROBE FURTHER. Ivan Getting published an autobiography entitled *All in a Lifetime, Science in the Defense of Democracy* (Vantage Press Inc., New York, 1989). For a detailed look at the workings of the Navstar Global Positioning Satellite System, see "Navstar: the all-purpose satellite," *IEEE Spectrum*, May 1981, pp. 35–40. ◆

Japan's nuclear power tightrope

A recent accident casts a pall over plans to add 40 plants in 20 years to the world's No. 4 nuclear complex

The timing could hardly have been worse. Early in February, just as Japan's nuclear energy program was regaining a degree of popular support after three years of growing opposition, an aging pressurized-water reactor at Mihama in western Japan sprang a leak in its primary cooling system. The event occasioned Japan's first nontest use of an emergency core-cooling system. It also elicited a forecast of "renewed public skepticism about nuclear power" from the Ministry of International Trade and Industry (MITI), the Government body responsible for promoting and regulating Japan's ambitious nuclear power program.

Public backing for this form of energy has always been a delicate flower in Japan, where virtually every school child visits the atomic bomb museums at Hiroshima and Nagasaki. Yet the country, which imports 80 percent of its energy and just about all its oil, is behind only the United States, France, and the Soviet Union in installed nuclear capacity. In fiscal 1989, which started in April, Japan's 39 nuclear power stations accounted for 25.5 percent of electricity generated—the largest contribution—followed by coal and natural gas. Twelve more plants are under construction.

MITI intends nuclear power stations to generate 43 percent of electricity by 2010. This will require 40 new plants, since demand for electricity is rising sharply. In the six months from April to September 1990, consumption was 8.8 percent higher than in the previous year—the largest growth since the 1973 oil crisis. In August, the peak month for demand, electric utilities had to ask large customers such as factories to cut consumption to avoid power cuts. Officials admit that increasing nuclear power's share of electricity generation will be very difficult. "It is not impossible, but extra efforts will be needed to achieve it," said Hideaki Tsuzuku, deputy head of nuclear policy at the Government's Science and Technology Agency.

Michael Cross Correspondent

The conjunction of the Gulf crisis with rising demand for electricity boosted the morale of nuclear engineers. In February, an election in Aomori Prefecture, site of Japan's enrichment and reprocessing plant, returned the sitting governor to power against an anti-nuclear-power challenger. "People understand that nuclear energy is essential for the peace of Japan," said Takeki Kawahito, superintendent of Kashiwazaki Kariwa power station in Niigata Province, which will be the world's largest concentration of commercial nuclear reactors in the late 1990s.

Then on Feb. 9, one of the 3260 U-shaped pipes in Mihama-2's steam generator produced the most dramatic breakdown in the history of nuclear power in Japan. According to a preliminary report by MITI, the accident began at 1:40 p.m. when Mihama-2 was in full power operation, with the sounding of a radiation alarm on the condenser vacuum pump gas monitor. Ten minutes later, while operators were reducing the reactor's power, instruments showed a drop in pressure and low water levels in the primary system, events that automatically triggered the reactor's emergency core-cooling system.

Construction is proceeding at a furious pace, aided by CAD/CAM systems and assembly modules

The emergency systems worked as designed, owner Kansai Electric Power Co. said, and brought the reactor to a halt. Inspection by television cameras and fiberscope revealed a crack in one of the tubes in use. About 20 metric tons of radioactive water leaked into the secondary system, some of which vented as steam through a safety valve into the outside air. MITI said that the amount of radioactivity released was "very small"—about 5 × 10^9 becquerels (0.1 curie), or about one-fiftieth of the plant's permitted annual emissions of radioactivity.

The prefectural government, however, complained that the plant's operators waited 90 minutes before notifying local authorities of abnormal levels of radiation.

Japan's boiling-water reactors have not been immune from malfunctions, either. On Jan. 1, 1989, a public holiday, the main recirculation pump at the No. 3 reactor at the Fukushima II Power Station, north of Tokyo, set off a vibration alarm. Vibrations continued for five days until the operator, Tokyo Electric Power Co. (Tepco), shut down the 1100-megawatt reactor. Inspection showed that a hydrostatic bearing had shattered, damaging the pump and spreading bolts, washers, and parts of the impeller plate throughout the reactor. The shutdown lasted 22 months while engineers removed debris from the pressure vessel, made repairs, and reassured anxious local people.

UNDER CONSTRUCTION. Fukushima II-3 is one of Tepco's newer boiling-water reactors. It began commercial operation in 1985. The utility operates a total of 13, at Fukushima and Kashiwazaki Kariwa, in Niigata Prefecture on the shores of the Japan Sea. Kashiwazaki Kariwa's third reactor (although numbered Kashiwazaki Kariwa 5) entered commercial service last September, a month ahead of schedule. Four more are in various stages of planning and construction. When complete, the power station's total capacity will be 8.2 million gigawatts, which Tepco says is the world's largest.

Construction is proceeding at a furious pace, aided by new techniques. One is the "large block construction method," in which modules weighing up to 400 tons are lifted into place by cranes.

New technology has also speeded the process of assembling steel reinforcement bars for concrete structures. Machines arrange the bars automatically, according to instructions from computer-aided design and manufacturing (CAD/CAM) systems. Other robots pour concrete and spray paint.

The most striking feature of the completed reactors is how little is visible above ground. The entire Japanese archipelago is prone to earthquakes. To reduce the risk of damage, the pressure vessels rest on bedrock 30 meters below sea level. In a major earthquake, sensors would automatically shut the plant down.

Two of the seven reactors planned for

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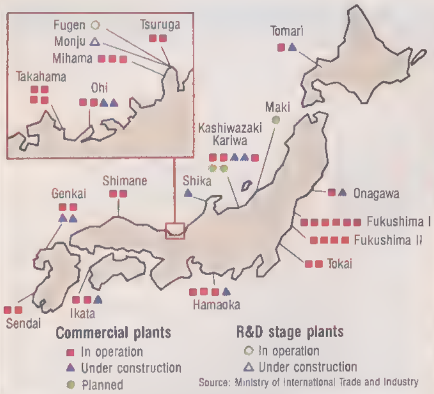


Present and planned reactor sites (above) will be augmented by fuel processing and a low-level waste depository being built at Rokkasho (below) on Japan's northernmost island, Hokkaido.

Michael Cross (photos)

This pressure vessel for a new Hitachi reactor at Kashiwazaki Kariwa plant 4 will go online in 1994.

Kashiwazaki Kariwa will be a showcase for the newly designed advanced boiling-water reactor, as it is called. It will have an electrical capacity of 1356 MW; compared with the present reactors' 1100 MW.

The main new feature is that the recirculation pump fits inside the pressure vessel, to reduce the risk of radiation leaks and lower the center of gravity for stability in earthquakes. The design is the result of collaboration between Tepco, General Electric Co., headquartered in Fairfield, Conn., and Toshiba Corp. and Hitachi Ltd.

Meanwhile, a rival consortium of Japanese companies is collaborating with Westinghouse Electric Corp., Pittsburgh, to develop an advanced pressurized-water reactor. This will have a generating capacity of 1300 MW (electrical), some 15 percent higher than today's reactors.

Both projects to improve light-water reactors grew in part from a collaborative R&D effort, known as the Improvement and Standardization Program, which MITI established in 1975. The 10-year project's goal was to reduce the downtime of reactors, the time taken to build plants—which spawned the techniques of modular construction—

1. Japan's nuclear power plants

Utility	Power plant	Reactor type[a]	Gross capacity, megawatts (electrical)	Prime contractor[b]	Start of commercial operation[c]
	In operation (40 units)				
Japan Atomic Power Co.	Tokai 1	GCR	166	GE/SC	7/66
	Tokai 2	BWR	1100	GE/Hitachi Ltd.	11/78
	Tsuruga 1	BWR	357	GE	3/70
	Tsuruga 2	PWR	1160	MHI	2/87
Hokkaido Electric Power Co.	Tomari 1	PWR	579	MHI	6/89
Tohoku Electric Power Co.	Onagawa 1	BWR	524	Toshiba Corp.	6/84
Tokyo Electric Power Co.	Fukushima I-1	BWR	460	GE	3/71
	Fukushima I-2	BWR	784	GE/Toshiba	7/74
	Fukushima I-3	BWR	784	Toshiba	3/76
	Fukushima I-4	BWR	784	Hitachi	10/78
	Fukushima I-5	BWR	784	Toshiba	4/78
	Fukushima I-6	BWR	1100	GE/Toshiba	10/79
	Fukushima II-1	BWR	1100	Toshiba	4/82
	Fukushima II-2	BWR	1100	Hitachi	2/84
	Fukushima II-3	BWR	1100	Toshiba	6/85
	Fukushima II-4	BWR	1100	Hitachi	8/87
	Kashiwazaki Kariwa 1	BWR	1100	Toshiba	9/85
	Kashiwazaki Kariwa 2	BWR	1100	Toshiba	9/90
	Kashiwazaki Kariwa 5	BWR	1100	Hitachi	4/90
Chubu Electric Power Co.	Hamaoka 1	BWR	540	Toshiba	3/76
	Hamaoka 2	BWR	840	Toshiba/Hitachi	11/78
	Hamaoka 3	BWR	1100	Toshiba/Hitachi	8/87
Kansai Electric Power Co.	Mihama 1	PWR	340	WE/MAPI	11/70
	Mihama 2	PWR	500	MAPI	7/72[d]
	Mihama 3	PWR	826	MHI	12/76
	Takahama 1	PWR	826	WE/MHI	11/74
	Takahama 2	PWR	826	MHI	11/75
	Takahama 3	PWR	870	MHI	1/85
	Takahama 4	PWR	870	MHI	6/85
	Ohi 1	PWR	1175	WE/MHI	3/79
	Ohi 2	PWR	1175	WE/MHI	12/79
Chugoku Electric Power Co.	Shimane 1	BWR	460	Hitachi	3/74
	Shimane 2	BWR	820	Hitachi	2/89
Shikoku Electric Power Co.	Ikata 1	PWR	566	MHI	9/77
	Ikata 2	PWR	566	MHI	3/82
Kyushu Electric Power Co.	Genkai 1	PWR	559	MHI	10/75
	Genkai 2	PWR	559	MHI	3/81
	Sendai 1	PWR	890	MHI	7/84
	Sendai 2	PWR	890	MHI	11/85
Power Reactor and Nuclear Fuel Development Corp. (PNC)	Fugen	ATR	165	Various	3/79
		Total gross capacity	31 645		

and employees' exposure to radiation.

The low doses of radiation to which workers are exposed are a symbol of Japanese skills in building and operating nuclear power stations. In fiscal 1989, the latest year for which figures are available, the average dose equivalent of workers in radiation control areas amounted to 1.6 millisieverts per worker, down by 0.1 mSv from the previous year. According to MITI's Agency of Natural Resources and Energy, this is the lowest figure on record. No worker in the nuclear power industry exceeded the legal limit of 50 mSv per year.

Plant managers say that design and good working practices are responsible for the low figures. As large and prestigious employers, utilities can attract a high caliber of recruits. Lifetime employment means that trained employees are unlikely to leave (and would not be hired by another utility) and ensures loyalty to the company. The whistleblower, for example, is almost unknown in Japan.

Signs of this conscientious approach to work are apparent throughout nuclear power stations. One example is the standard of cleanliness. Not only radiation control areas but turbine halls, canteens, and toilets are spotless. The controllers themselves are long-service company personnel (the only women are cleaners or smartly dressed tour guides). A shift leader would have at least 10 years' experience.

Loyalty to the company is at least as strong in the major contractors. Hitachi and Toshiba are among Japan's most prestigious companies and recruit for life from the country's top campuses, led by Tokyo University. Companies normally hire engineering and scientific staff after a bachelor's degree, to be supplemented with many years of in-house training. Engineers are treated as "all-rounders," expected to learn new fields as required. One nuclear engineer, after years working on the metallurgy of pressure-vessels, found himself reassigned to his company's biotechnology division.

AT THE TOP. The energy complex run by this elite group of workers is administered by a tripartite alliance of Government departments, electric utilities, and engineering contractors. The lead agency is MITI. It is responsible for approving the siting, design, and operation of nuclear power plants. It also has powers to set electricity prices and, through the mechanism of "administrative guidance," to direct private companies. The Science and Technology Agency is responsible for nuclear research. As for Japan's electric utilities, there are nine of them, each a privately owned local monopoly. All contribute to private consortia formed, under Government guidance, to handle different nuclear technologies.

One of these is the Japan Atomic Power Co., which ordered Japan's first power reactor, a gas-cooled type of the British Magnox design, in 1959. It is still running.

By the mid-1960s, Japan's electric utilities had switched to U.S. technology, the light-water reactor, for their future plans. The nine companies fell into two camps. Tepco, the world's largest private electricity utility, with revenues of some 4.2 trillion yen (US $32.7 billion), led one group. It chose a boiling-water reactor, from General Electric, which Hitachi and Toshiba built under license. The second-largest electricity generator, Kansai Electric Power, led a group choosing the pressurized-water reactor, which was built by Mitsubishi Atomic Power Industries and other Mitsubishi companies under license from Westinghouse.

Japan's first commercial boiling-water reactor, Tsuruga 1, in Fukui Prefecture, West Japan, went critical in October 1969. The first commercial pressurized-water reactor, Mihama-1, also in Fukui, followed a year later. Today, the second type slightly outnumbers the first in Japan and forms the majority of plants under construction.

Japan, however, remains dependent on the outside world for several crucial parts of the nuclear cycle: it has few known sources of uranium, and it exports spent fuel to Britain and France for reprocessing at those countries' facilities at Sellafield and Cap La Hague ["Nuclear waste: the challenge is global," *IEEE Spectrum*, July 1990, pp. 18–24].

REPROCESSING AT ROKKASHO. This dependency has spurred plans to round out the fuel cycle, starting with a gigantic plant under construction near the village of Rokkasho, Aomori Prefecture, at the far northern end of Honshu. The site, which covers nearly 400 hectares, will house plants for enriching uranium and storing and reprocessing fuel as well as a depository for low-level nuclear waste, now stored mostly at nuclear power stations. The whole complex will cost some 840 billion yen (US $6.5 billion).

Fuel enrichment and low-level waste storage at Rokkasho are the responsibility of Japan Nuclear Fuel Industries Co., a private concern owned by the nine electric power utilities but with three nuclear engineering companies and several financial institutions holding a minority stake. Under international nonproliferation rules, Japan had to develop its own enrichment technology, a centrifugal process. The program began in the 1960s, with a pilot plant in Ningyo, Okayama Prefecture, West Japan. The Government's Science and Technology Agency and private companies are also studying laser and chemical enrichment technologies.

Rokkasho's enrichment plant will cost 180

Utility	Power plant	Reactor type[a]	Gross capacity, megawatts (electrical)	Prime contractor[b]	Start of commercial operation[c]
Under construction (12 units)					
Hokkaido Electric	Tomari 2	PWR	579	MHI	(6/91)
Tohoku Electric	Onagawa 2	BWR	825	Toshiba	(7/95)
Tepco	Kashiwazaki Kariwa 3	BWR	1100	Toshiba	(7/93)
	Kashiwazaki Kariwa 4	BWR	1100	Hitachi	(7/94)
Chubu Electric	Hamaoka 4	BWR	1137	Toshiba/Hitachi	(9/93)
Hokuriku Electric Power Co	Shika	BWR	540	Hitachi	(3/93)
Kansai Electric	Ohi 3	PWR	1180	MHI	(12/91)
	Ohi 4	PWR	1180	MHI	(2/93)
Shikoku Electric	Ikata 3	PWR	890	MHI	(3/95)
Kyushu Electric	Genkai 3	PWR	1180	MHI	(3/94)
	Genkai 4	PWR	1180	MHI	(7/97)
PNC	Monju	FBR	280	—	—
Total gross capacity			11 171		
Planned (3 units)					
Tohoku Electric	Maki 1	BWR	825	—	(2000)
Tepco	Kashiwazaki Kariwa 6	ABWR	1356	—	(7/96)
	Kashiwazaki Kariwa 7	ABWR	1356	—	(7/97)
Total gross capacity			3537		

Source: Japan Atomic Industrial Forum

a ABWR = advanced boiling-water reactor; ATR = advanced thermal reactor; BWR = boiling-water reactor; FBR = fast-breeder reactor; GCR = gas-cooled reactor; PWR = pressurized-water reactor.

b GE = General Electric Co.; MAPI = Mitsubishi Atomic Power Industries Inc.; MHI = Mitsubishi Heavy Industries Inc.; SC = Shimizu Corp.; WE = Westinghouse Electric Corp.

c Scheduled starting dates are in parentheses.

d Suspended February 1991.

2. Japan's advanced and current boiling-water reactors

Parameter	Advanced	Current (BWR-5)
Electrical output, megawatts	1356	1100
Reactor thermal output, MW	3926	3293
Reactor pressure, kilograms per square centimeter	73.1	71.7
Steam flow, metric tons per hour	7480	6410
Feed water temperature, degrees Celsius	215	215
Core flow, kilograms per hour	52×10^6	48×10^6
Number of fuel assemblies	872	764
Number of control rods	205	185
Core average power density, kilowatts per liter	50.6	50.0

Source: *Atoms in Japan*

billion yen (US $1.4 billion) and be capable of handling 1500 tons of uranium a year—some 30 percent of Japan's consumption—by the end of the century. It is due to begin operation in September, five months behind the original schedule. Officials say the main cause of the delay was the decision to suspend installation of the centrifugal separator for four months following the election in November 1989 of a Rokkasho mayor who opposed the project.

Japan's nuclear power plants have accumulated about half a million 200-liter drums of such waste, mostly asphalt, clothing, and liquids. Japan Nuclear Fuel Industries applied to the Government in 1988 for permission to start building the low-level depository at Rokkasho, which could eventually store 600 000 drums. The Government withheld its approval until last November, though—until after the company had made several changes to improve access to stored drums. The site will accept its first drums in late 1992, more than a year behind schedule.

Responsibility for the reprocessing plant at Rokkasho belongs to a separate consortium, Japan Nuclear Fuel Service Co. (though its shareholders are mostly identical to those of Japan Nuclear Fuel Industries). It hopes to begin reprocessing in 1997, but is still awaiting approval to begin construction. The country's only reprocessing now takes place at a pilot plant in Tokai, Ibaraki Prefecture, near Tokyo. Since 1977 it has reprocessed some 400 tons of fuel. Rokkasho will handle 800 tons a year.

Former Prime Minister Yasuhiro Nakasone once described Aomori as "Japan's nuclear peninsula." Apart from Rokkasho, it also houses the port built for Japan's first and only nuclear ship, the *Mutsu*. The region has become the focus of opposition to nuclear power in Japan, which emerged on a wide scale for the first time after the 1986 Chernobyl disaster. Among the 12 000 inhabitants of Rokkasho village itself, the issue dominates a bitter political debate.

The reprocessing plant's output will supply Japan's plutonium reactors. This has raised fears over safety at home and abroad. A prototype fast-breeder reactor, named Monju, is to start operating in Fukui Prefecture in October 1992. This 714-MW (thermal) sodium-cooled reactor is a midway stage between the country's first prototype breeder, Joyo, and full-scale commercial fast-breeder reactors. Its fuel will be an oxide of plutonium and uranium.

Another research program is using the so-called advanced thermal reactor to develop ways to fuel light-water reactors with plutonium. A prototype of the reactor, called Fugen, has been operating near Tsuruga City, Fukui Prefecture, since 1978. Its purpose is to evaluate the performance and safety of plutonium-uranium metal oxide fuel. "Proper containment and radiation control technologies make safe use of plutonium feasible," said the Government's 1990 Report on Atomic Energy. Commercial reactors will begin to use plutonium in the late 1990s.

RIGHTS OF PASSAGE. Until the reprocessing plant at Rokkasho comes on stream, Japan's plutonium program will depend on fuel reprocessed under commercial contracts in England and France. The need to return this plutonium to Japan has involved Tokyo in a series of international conflicts.

The original proposal—transport by air—foundered because of objections in the United States. (The fuel originated from U.S. uranium, so is subject to U.S. controls. Also, flights between Europe and Japan would have passed over U.S. territory.) The alternative, transport by sea, raised fears of hijacking by terrorists or unscrupulous governments. Tokyo agreed to provide an armed escort, which was opposed because it appeared to breach the policy of not deploying Japanese troops overseas.

The solution was to give the job of escorting plutonium to the country's Maritime Safety Agency, a coastguard force. An armed escort ship is now under construction, at a cost of 20 billion yen (US $154 million). Shipments are due to begin in fall 1992.

One stage in the nuclear fuel cycle remains to be tackled in Japan—disposal of high-level nuclear wastes. The Government's policy is to vitrify waste—a process akin to sealing it in glass marbles—then store it for 30 to 50 years underground and finally bury it at a depth of several hundred meters. This is the responsibility of yet another entity, a private consortium called the Power Reactor and Nuclear Fuel Development Corp. Studies on geological disposal are taking place at a site near Horonobe, in the center of the northern island of Hokkaido.

LOOKING ASKANCE. Officials stress that this does not mean that Horonobe will be the site of the depository itself. But local residents are more skeptical, and Horonobe has become another focus for the nationwide antinuclear movement.

Before the emergency shutdown at Mihama, opinion polls showed that most Japanese express concern about nuclear power yet regard it as essential. Officials in Government and industry say that the job of promoting nuclear energy in Japan is mainly one of explanation and education. However, Kazuhisa Mori, executive managing director of the Japan Atomic Industrial Forum, through which 800 companies promote nuclear energy, bemoaned that "the more serious a person is about energy and the environment, the more likely he is to oppose nuclear energy."

Mori is also puzzled that opponents of nuclear power do not believe that MITI and the utilities are telling the whole story. "One feeling that emerges in polls is that the industry is hiding something," he said. "Obviously there are commercial secrets and locations of sensitive materials that cannot be released." Otherwise, he insisted, "we are completely open."

> Rokkasho will provide low-level waste storage and a tripling of Japan's reprocessing capability

TO PROBE FURTHER. The Japan Atomic Industrial Forum publishes a monthly English-language magazine called *Atoms in Japan*. It is available from the forum at: 1-13-1 Shinbashi, Minato-ku, Tokyo 105, Japan; (81+3) 3508 2411; fax, 3508 2094.

Government agencies concerned with nuclear energy are the Science and Technology Agency, 2-2-1 Kasumigaseki, Chiyoda-ku, Tokyo 100, Japan [contact the Office of Atomic Energy Policy Research, (81+3) 3581/5197] and the Ministry of International Trade and Industry, 1-3-1 Kasumigaseki, Tokyo 100 [contact the Agency of Natural Resources and Energy, (81+3) 3501-1511].

A prominent opposition group that publishes information in English is the Citizen Nuclear Information Center, 3F Watenabe Building, 2-23-22 Higashi Ueno, Taito-ku, Tokyo 110, Japan.

ABOUT THE AUTHOR. Michael Cross is a science and technology correspondent who formerly headed *New Scientist* magazine's bureau in Tokyo. ◆

The engineer at large

Contest seeks ideas to enable the disabled

There's a US $10 000 first prize out there for the best ideas, systems, devices, or computer programs for helping persons with disabilities. The $10 000, as well as 100 other prizes and awards, is being offered by the Johns Hopkins National Search for Computing Applications to Assist Persons with Disabilities. U.S. residents are invited to submit entries in four major areas: employment, independent living, education, and leisure.

The search, supported by grants from the National Science Foundation and MCI Communications Corp., both in Washington, D.C., will be conducted in collaboration with leading rehabilitation, business, educational, and professional organizations in the technical and disability communities. The effort also expects to attract corporate sponsors.

Contests in each of the 10 standard Federal U.S. regions will be used to attract competitors nationwide. Each region will present its own fair on Dec. 7, 1991, where award presentations will be made and hundreds of inventions displayed. The culmination of the search will be a national fair and awards ceremony at the Smithsonian Institution in Washington, D.C., in February 1992.

Paul Hazan (SM) of the Applied Physics Laboratory, Johns Hopkins University, Laurel, Md., leads the search. Hazan directed a similar program in 1981 that yielded 8000 participants and hundreds of inventions, many of which eventually became standard equipment for thousands of persons with disabilities.

One invention, for example, led to Braille 'N Speak, a pocket-sized input terminal marketed by Blazie Engineering Co. of Street, Md., that accepts keyed-in Braille shorthand and outputs spoken words or ASCII code for input to a word processor. Another invention became the Eyetyper 300, an eye-gaze–controlled keyboard system for severely paralyzed and speech-impaired individuals. Marketed by Sentient Systems Technology Inc., Pittsburgh, the device, by focusing a camera at the person's eye, allows words to be selected from those displayed on a computer screen.

Hazan expects the present search to make an even greater impact than the first one. "In 1981, there were only 200 000 personal computers in the hands of Americans," Hazan said. "Today there are about 20 million—almost a 100-fold increase." Thus, the pool of creative people who are computer literate is far larger and this should generate many more good ideas, Hazan added.

He pointed out that public schools in the United States have almost a million computers devoted to special education. Therefore, a single, well-designed piece of educational software could help many thousands of students with learning problems.

Giving businesspeople access to the inventions is another goal of Hazan and the Applied Physics Laboratory. To this end, a "future directions" workshop at the laboratory will immediately follow the national awards ceremony. The workshop will present marketable entries to manufacturers and disability group leaders. Computer networking systems also will be used to disseminate information, and a nationally televised program will bring the results of the search to the public.

A TV workshop is also planned for April 6 in the United States to be broadcast over the Black College Satellite Network and 250 cable stations. The program will present details of the contest and answer phoned-in questions. Deadline for entries is Aug. 23, 1991. *Contact: Personal Computing to Assist Persons with Disabilities, Box 1200, Laurel, Md. 20723.*

NSPE picks engineering feats

Its pick of the top U.S. engineering achievements of 1990 was announced recently by the National Society of Professional Engineers (NSPE), Washington, D.C. Conspicuous among them is the recovery program for the Three Mile Island Unit 2 (TMI-2) nuclear power plant. According to NSPE, the program pointed the way for the nuclear industry in hazardous waste cleanup. Eight other projects will also receive the society's 25th annual awards for Outstanding Engineering Achievement

Kazu

Two winners of particular interest to electrical engineers are the prefabricated Sidney A. Murray Jr. Hydroelectric Station, situated

The engineer at large

140 kilometers northwest of Baton Rouge, La., and the Downtown Seattle (Wash.) Transit Project—actually an electric-trolley tunnel and station system.

The March 18, 1979, accident at TMI-2 was extremely serious. Reactor fuel melted. Fission products escaped into plant buildings. A massive amount of molten fuel flowed from the reactor core into the rest of the reactor vessel. To recover from the accident, engineers had to stabilize the plant, decontaminate it, and remove the damaged reactor fuel to a secure location. Each of these steps presented an unprecedented engineering challenge, according to NSPE. The recovery effort, which lasted for 11 years and cost over US $975 million, was led by General Public Utilities Nuclear Corp., Parsippany, N.J., and Bechtel Group Inc., San Francisco.

The accident and ensuing recovery effort yielded the only data yet available on core damage progression, fission product release, vessel margin-to-failure, and pressure conditions for a full-scale reactor system. At present, the plant is in a stable and safe condition, and the nuclear industry has new technology and a data and experience base for engineers and managers to apply in the future, said NSPE.

The Murray Hydroelectric Station, the first such installation in Louisiana, is the largest prefabricated power plant in the world. Eight turbines and ancillary generating equipment were built in Europe. The 24 000-metric-ton power plant itself was built 333 kilometers down river at a New Orleans shipyard and towed up the Mississippi River to the foundation constructed at the project site. The 192-megawatt facility will provide electricity for 200 000 people and has a life expectancy of over 100 years.

The heart of the Seattle transit project is a 21-km electric trolleybus tunnel through the city's center, the only one in the world built exclusively for electric buses. The $459 million project also includes five stations and a surface electric-bus system.

The two-block-long stations accommodate up to four buses, which operate under diesel power outside downtown Seattle but switch to electric traction before entering the tunnel and the downtown core of the city. What's more, station platforms and tunnel grades and turning radii were all designed with a future light-rail system in mind.

Other winners of the NSPE engineering achievement awards included a system for supplying diesel fuel from ship to shore in a battlefield environment, and an unfinished nuclear power plant in Midland, Mich., that was converted to natural-gas–fueled power generation.

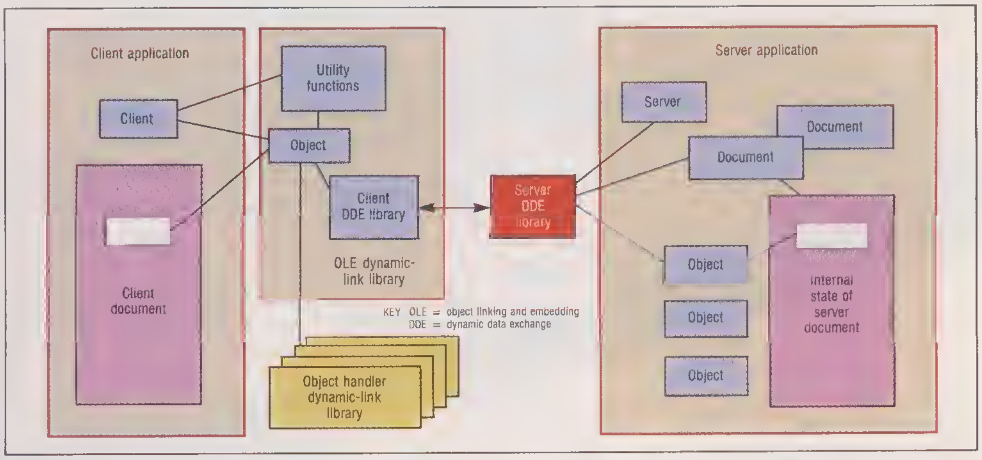
COORDINATOR: Alfred Rosenblatt

Program notes

Editing made easy

Complex documents, like complex software, are typically created from smaller segments. But building complex documents is the harder job, because the document segments are often not in the same format and must then be translated into a common format first.

Software engineers now use object-oriented programming techniques to build complex documents [see "The case for object-oriented databases," February 1991, pp. 44–47]. Treating the segments as objects with data in a specified format has several advantages.



OLE server applications like drawing and spreadsheet programs store objects in several libraries. The objects are linked by DDE to OLE libraries for client applications like word-processing programs.

First, if the segment is embedded in the larger document as an object, none of the information in the segment is eliminated. When a vector graphics drawing, say, is translated to a bit map in the larger document, it cannot be enlarged without loss of resolution; but when a vector graphical object is embedded in the larger document, there is no loss of resolution when it is scaled. Second, if the segment is linked to the larger document as an object, changes in the segment are hot-linked to the larger document. Thus, when a spreadsheet containing a table is linked to the larger document, changes in the table automatically appear in the larger document because the latter reads the current spreadsheet, not an older version.

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Calendar

(Continued from p. 14D)

Larry Coldren, University of California, Department of Electrical Engineering and Computer Engineering, Santa Barbara, Calif. 93106; 805-893-4486.

Eighth IEEE Pulsed Power Conference (ED); June 17–19; Sheraton Island Harbor Hotel, San Diego, Calif.; Roger White, Maxwell Laboratories Inc., 8888 Balboa Ave., San Diego, Calif. 92123; 619-576-7884.

University/Government/Industry Conference (ED); June 18–20; Melbourne Holiday Inn, Oceanside, Fla.; Thomas Sanders, Florida Institute of Technology, 150 W. University Blvd., Melbourne, Fla. 32901; 407-768-8000, ext. 8769/8763.

Joint Magnetism and Magnetic Materials-Intermag Conference (MAG); June 18–21; Pittsburgh Hilton, Pittsburgh; Diane Suiters, Conference Coordinator, 655 15th St., N.W., Suite 300, Washington, D.C. 20005; 202-639-5088; fax, 202-347-6109.

SSIT Interdisciplinary Conference (SSIT); June 21–22; Ryerson Polytechnical Institute, Toronto, Ont.; Diane Falkner, Program Director Conferences, Ryerson Polytechnical Institute, 350 Victoria St., Toronto, Ont., Canada M5B 2K3; 416-979-5184; fax, 416-979-5148.

International Conference on Communications (COMP); June 23–26; Denver Technical Center, Hyatt and Sheraton, Denver, Colo.; Russell Johnson, Western-Telecommunications Inc., 4643 S. Ulster St., Suite 400, Denver, Colo. 80237; 303-721-5650.

Antennas and Propagation Society International Symposium and URSI National Radio Science Meeting (AP); June 23–27; University of Western Ontario, London, Ont., Canada; A. R. Webster, Faculty of Engineering Science, University of Western Ontario, London, Ont., Canada N6A 5B9; 519-679-6294.

International Symposium on Information Theory (IT); June 23–28; Budapest Conference Center, Budapest, Hungary; Anthony Ephremides, Department of Electrical Engineering, University of Maryland, College Park, Md. 20742; 301-405-3641.

Power Electronics Specialist Conference– PESC '91 (PEL); June 24–28; Massachusetts Institute of Technology (MIT), Cambridge; Martin Schlecht, MIT, Room 39-553, Cambridge, Mass. 02139; 617-253-3407.

(Continued on p. 86F)

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Calendar

(Continued from p. 86B)

Transducers '91: International Solid-State Sensors and Actuators Conference (ED); June 24–28; Hyatt Regency Hotel, San Francisco; Richard S. Muller, 497 Cory Hall, Berkeley Sensor and Actuators Center, University of California at Berkeley, Berkeley, Calif. 94720; 415-642-0614.

American Control Conference–ACC '91 (CS); June 26–28; Boston; Timothy Johnson, General Electric Co., Research and Development, KWD 217, Box 8, Schenectady, N.Y. 12345; 518-387-5096.

JULY

28th IEEE Nuclear and Space Radiation Effects Conference (IEEE Nuclear and Plasma Sciences Society); July 15–19; Town and Country Hotel, San Diego, Calif.; James R. Schwank, Sandia National Laboratories, Division 2144, Box 5800, Albuquerque, N.M. 87185; 505-846-8485.

Power Engineering Society Summer Meeting (PE); July 28–Aug. 1; Marriott Hotel, San Diego, Calif.; T.M. Winter, San Diego Gas & Electric Co., 101 Ash St., Box 1831, San Diego, Calif. 92112; 714-232-4252.

AUGUST

26th Intersociety Energy Conversion Engineering Conference–IECEC '91 (ED); Aug. 3–9; Boston Marriott Hotel, Boston; Patrick Bailey, Lockheed Missiles & Space Co., 1111 Lockheed Way (59-32-535), Sunnyvale, Calif. 94088; 408-756-4268.

Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits (ED); Aug. 5–7; Cornell University, Ithaca, N.Y.; R.J. Trew, North Carolina State University, Electrical and Computer Engineering Department, Box 7911, Raleigh, N.C. 27695; 919-737-2336.

International Symposium on Electromagnetic Compatibility–EMC '91 (EMC et al.); Aug. 13–15; Hyatt Cherry Hill Hotel, Cherry Hill, N.J.; Henry W. Ott, 45 Baker Rd., Livingston, N.J. 07039; 201-386-6660.

Workshop on the Future of Electronic Power Processing and Conversion (IA); Aug. 28–29; Kruger National Park, South Africa; William Portnoy, Texas Tech University, Department of Electrical Engineering, Box 4439, Lubbock, Texas 79409-3102; 806-742-3533.

SEPTEMBER

Bipolar Circuits and Technology Meeting (ED); Sept. 9–10; Minneapolis Marriott Hotel, Minneapolis, Minn.; John Shier, 2401 E. 86th St., Bloomington, Minn. 55425; 612-851-5228.

Petroleum and Chemical Industry Technical Conference (IA); Sept. 9–11; Royal York, Toronto; Barry Wiseman, Reliance Electric Co., 5220 Creekbank Rd., Mississauga, Ont., Canada L3W 1X1; 416-625-8112.

Third International Conference on Microstructures in Biological Research (ED); Sept. 9–12; Fort McGruder Inn and Conference Center, Williamsburg, Va.; Martin Peckerar, Naval Research Laboratory, 4555 Overlook Avenue, S.W., Washington, D.C. 20375-5000; 202-767-3150.

Seventh Multidimensional Signal Processing Workshop (SP); Sept. 23–25; Whiteface Inn, Lake Placid, N.Y.; John Woods, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, N.Y. 12181; 518-276-6079.

18th International Conference on Computers in Cardiology (COMP et al.); Sept. 23–26; Venice, Italy; Corso Stati Uniti 4, 35020 Padova, Italy; (39+49) 829 5702.

International Symposium on Gallium Arsenide and Related Compounds (ED); Sept. 23–26; Seattle, Wash.; L. Ralph Dawson, Sandia National Laboratories, Division 1144, Albuquerque, N.M. 87185; 505-845-8920.

Fourth Annual International Application Specific Integrated Circuits Conference and Exhibit (IEEE Rochester et al.); Sept. 23–27; Rochester Riverside Convention Center, Rochester, N.Y.; Kenneth W. Hsu, Department of Computer Engineering, Rochester Institute of Technology, Rochester, N.Y. 14623; 716-475-2655; fax, 716-475-6879.

Industry Applications Society Conference (IA); Sept. 28–Oct. 4; Hyatt Regency, Dearborn, Mich.; William Moylan, Moylan Engineering Associates, 13530 Michigan Ave., Dearborn, Mich. 48126; 313-582-9880.

OCTOBER

International Joint Power Generation Conference–IJPGC '91 (PE); Oct. 6–9; Town and Country Hotel, San Diego, Calif.; M. Scalice, ASME, 345 E. 47th St., New York, N.Y. 10017; 212-705-7053.

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Recent books

(Continued from p. 14)

Automated Mainframe Management: Using Expert Systems with Examples from VM and MVS. *Seadle, Michael S.*, McGraw-Hill, New York, 1990, 394 pp., $44.95.

The Consultant's Manual. *Greenbaum, Thomas L.*, John Wiley, New York, 228 pp., $49.95.

Deterrence and the Revolution in Soviet Military Doctrine. *Garthoff, Raymond L.*, Brookings Institution, Washington, D.C., 1990, 210 pp., $29.95.

LAN Manager Programmer's Reference. *Microsoft Corporation*, Microsoft Press, Redmond, Wash., 1990, 878 pp., $39.95.

Weibull Radar Clutter. *Sekine, Matsuo, and Mao, Yuhai*, Peter Peregrinus, London, 1990, 190 pp., $69.

The Universe and Its Origins. *Singer, S. Fred*, Paragon House, New York, 1990, 287 pp., $34.95.

Knowledge-based Systems for Industrial Control. Ed. *McGhee, J., Grimble, M.J., and Mowforth, P.*, Peter Peregrinus, London, 1990, 345 pp., $75.

16/32-Bit Microprocessors 68000/68010/68020: Software, Hardware, and Design Applications. *Subbarao, Wunnava V.*, Macmillan Publishing, New York, 1991, 454 pp., $45.

A C++ Toolkit. *Shapiro, Jonathan S.*, Prentice-Hall, Englewood Cliffs, N.J., 1991, 231 pp., $26.

VM & CMS: Performance and Fine Tuning. *Savit, Jeffrey*, McGraw-Hill, New York, 1990, 271 pp., $44.95.

Video Cameras and Camcorders. *Hobbs, Marvin*, Prentice-Hall, Englewood Cliffs, N.J., 1989, 321 pp., $40.

Metres to Microwaves. *Callick, E.B.*, Peter Peregrinus, London, 1990, 240 pp., $75.

AS/400: Concepts and Facilities. *Baritz, Tony, and Dunne, David*, McGraw-Hill, New York, 1990, 279 pp., $39.95.

Managing Business Transactions. *Rubin, Paul H.*, Free Press, New York, 1990, 181 pp., $27.95.

EGA/VGA: A Programmer's Reference Guide, 2nd edition. *Kliewer, Bradley Dyck*, McGraw-Hill, New York, 1990, 371 pp., $24.95.

Object-Oriented Databases with Applications to Case, Networks, and VLSI CAD. Ed. *Gupta, Rajiv, and Horowitz, Ellis*, Prentice-Hall, Englewood Cliffs, N.J., 447 pp., $49.

Object-Oriented Programming with Smalltalk/V. *Savic, Dusko*, Ellis Horwood, London, 1990, $59.95, 340 pp.

Engineering in History. *Kirby, Richard Shelton, et al.*, General Publishing, Toronto, 1990, 530 pp., $13.95.

Software Conflict. *Glass, Robert L.*, Prentice-Hall, Englewood Cliffs, N.J., 1991, 248 pp., $28.

HDTV: Advanced Television for the 1990s. *Benson, K. Blair, and Fink, Donald G.*, McGraw-Hill, New York, 1990, 370 pp., $39.95.

Statics of Deformable Solids. *Bisplinghoff, Raymond L., Mar, James W., and Pian, Theodore H.H.*, Dover Publications, New York, 322 pp., $10.95.

Verifying and Validating Personal Computer-Based Expert Systems. *Bahill, A. Terry*, Prentice-Hall, Englewood Cliffs, N.J., 1991, 205 pp., $29.

Program notes

used limited object-oriented programming techniques in Windows. The Windows Clipboard, a utility that captures highlighted text or graphics in a Windows application program, embeds segments created by Windows applications in other documents since it transfers both format and data. Also, Windows applications can use dynamic data exchange (DDE) to hot-link data in one application with another, so that data from one program is automatically copied to another.

Now to complement the Clipboard and DDE, object linking and embedding (OLE) is being added. OLE outdoes the Clipboard and DDE in several respects. First, it extends the object concept by adding a predigested form of the segment in the generic Metafile format, a device-independent pictorial description of the object. This reduces the overhead associated with converting objects in foreign formats to a displayable format. Second, OLE is supported by an extended Windows dynamic-link library (DLL), functions supplied by Microsoft that allow applications to deal with objects at a high level. These functions reduce writing the code required to manipulate objects to a few lines that call these functions. This makes manipulating the segments easier [see illustration, p. 86].

When OLE-based versions of Windows word processors become available, documents using OLE will be much easier to edit and revise than documents that use the Clipboard and DDE. Scrolling through the documents will be much faster. It will also become possible to select, edit, and save graphical or spreadsheet segments within a document in their native format—all while in that document.

Microsoft has also announced plans for OLE on the Macintosh when System 7 is released so OLE will be a cross-platform capability. *Contact: Katherine Hinsch, Microsoft Corp., 1 Microsoft Way, Redmond, Wash. 98052-6399; 206-882-8080; or Claire Lematta, the Waggener Group, 6915 S.W. Macadam Ave., Room 300, Portland, Ore. 97219; 503-245-0905; or* **circle 112.**

Games as teachers

As home computers with high-resolution color graphics become the norm, high-resolution graphical games are being written for home computers. Card games like Solitaire and strategy games like Reversi often come free with another program, while arcade games like Tetris are available for the cost of a fancy dinner.

Educational games with high-resolution graphics are also available for the home computer market. Often, the authors of these programs have made the graphics an integral part of the game, rather than an add-on. The Carmen Sandiego games from Broderbund Software Inc., San Rafael, Calif., for example, use high-resolution graphics to teach social studies skills. The student's mission is to catch Carmen and her gang of globe-trotting thieves before the warrant for their arrests expires. Text clues like "She converted her money to pesos" and "He left in a limousine flying a blue and yellow flag" complement a map showing possible destinations. And, when the destination is correctly identified, Keystone Kops chase the thieves across the screen and haul them off to jail. It's easier to learn social studies from Broderbund than from old Mrs. Bundy!

The most difficult task in creating an educational game is identifying a fun activity that can be linked to the skill being taught. Finding amusing ways to teach basic engineering concepts is hard, though. Fame and fortune await the first individual who can identify a fun activity that will teach binary arithmetic or Boolean algebra. Any good ideas?

COORDINATOR: Gadi Kaplan
CONSULTANTS: John Kellum, Intergraph Advanced Processor Division; Stuart Feldman, Bellcore, Computer Systems Research.

EEs' tools & toys

CD ROM stores a heap of abstracts

Given the seemingly exponential accumulation of journals, conferences, and papers, isolating the information you need can be a labor of Hercules. So Engineering Information Inc. has scooped up a million abstracts of articles published in the past 10 years onto a CD-ROM database that it calls Ei EEDisc. The compact disc (CD) homes in on such areas as computer science, magnetics, optics, and electrical engineering, and includes many journals and conferences in its sweep.

The same information can also be dug up by means of many online services, but the bill can be big if many searches are done. It may make better economic sense to use a CD ROM for most searches and reserve the online service for finding abstracts published after the CD was made. Since the Ei EEDisc is offered in conjunction with Dialog Information Services, Palo Alto, Calif., it facilitates this approach. After the CD search, the researcher can use the Dialog OnDisc software to dial up and search Dialog's Compendex Plus database without reentering the search criteria.

A PC with a CD-ROM drive and Microsoft extensions is required. The CDs are published quarterly. A one-year subscription costs US $6750 for 10 years of abstracts or $3850 for five years. *Contact: Marcia Kaufman, Engineering Information Inc., 345 East 47 St., N.Y., N.Y. 10017-2387; 212-705-7616; or* **circle 100.**

SOFTWARE

Transition in Japan

Entering a new market is never a cinch, and Japanese markets are singularly challenging. U.S. software companies in particular have fought shy of them, for lack of knowledge of their trends and distribution channels. But much of the necessary information has been published in a 300-page report titled *Japan's Personal Computer Software Market.*

The report has been compiled by the Japan Personal Computer Software Association (JPSA), Tokyo, a group of Japanese software and hardware manufacturers. It discusses hardware, software, and distribution trends during 1989 and 1990, newly developed software and platforms, and the results of Japanese Government and JPSA studies. It also forecasts the trends of market segments over the immediate future.

In the past, Japanese end-users have preferred custom software implementations over standardized packages. Now, according to Norton Greenfeld, president of the report's English language distributor, Implements Inc., the market is shifting as more Japanese realize that using standard software packages has advantages. There are ample opportunities to enter this market now while it is in transition, especially since many Japanese consider foreign software superior to what is currently available in Japan, Greenfeld said.

The report costs US $495. *Contact: Norton Greenfeld, Implements Inc., 6 Brook Trail Rd., Wayland, Mass. 01778-3706; 508-358-5858; or* **circle 102.**

CAD for student analog design

Few students are willing to shell out US $1000 or more to buy one of the computer-aided design (CAD) tools that are at the disposal of many engineers. Still, they might consider the student edition of Micro-CAP III, licensed by Spectrum Software, Sunnyvale, Calif. (no relation to this magazine).

Unlike its big brother, the student edition will analyze circuit diagrams of at most 30 nodes. Nor does it do parameter estimation or Monte Carlo analysis, or directly support a plotter. Apart from that, it contains all of the design and analysis functions (such as ac, dc, and transient response), and has a graphical interface, a library of electronic symbols that can be customized, and some educational material that does not come with the professional version.

For under $50 a student can put this product on any IBM PC or compatible equipped with 640K of RAM and DOS 3.0 or later. *Contact: Addison-Wesley Publishing Co., 1 Jacob Way, Reading, Mass. 01867; 617-944-3700; or Kevin Howat at 415-594-4479; or* **circle 103.**

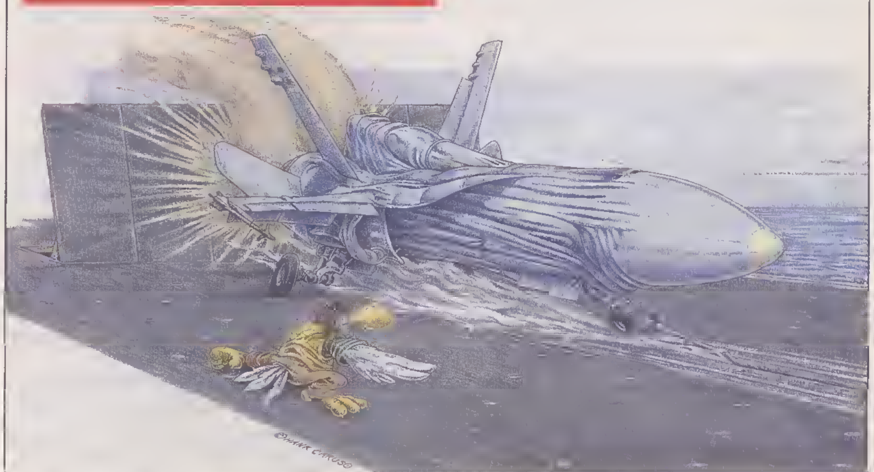
AUTOMATION

A middleman for CAD/CAM operators

Companies that hire operators of computer-aided design and manufacturing (CAD/CAM) workstations must determine a prospective employee's qualifications in a cost-effective manner. Conversely, operators seeking a job must be able to convince prospective em-

TOYS

Hank Caruso



Plane-of-the month calendar depicts F-18A Hornet awaiting catapult.

Airplanes personified

If through either your work or military service you've developed an emotional attachment to aircraft, you may want a copy of Hank Caruso's Aerocatures Calendar for 1991. An artist, as well as an engineer at Westinghouse Electric Corp. in Baltimore, Md., Caruso has expressed his attachment by drawing caricatures of 12 mostly military aircraft and giving them human-like personalities. Some in the plane-of-the-month calendar, like the P-38 Lightning and the Hurricane of Battle of Britain fame, go back to World War II. Others, like the A-6E Intruder and F-117A Stealth, are much more recent.

In black-and-white and a color cover, the calendars are US $8 each plus $2.50 for shipping in the United States and Canada. Discount prices are available for 25 or more. *Contact: Forefeathers Enterprises, Box 578, Glen Burnie, Md. 21060; or* **circle 101.**

EEs' tools & toys

ployers that they are qualified. But testing the expertise of an applicant can be a slow and expensive business. The National Association of CAD/CAM Operators (NACO), a nonprofit organization, thinks it can mediate with a procedure it has developed for testing and certifying CAD/CAM operators.

Members are required to submit a detailed resume, which NACO verifies for accuracy by contacting the applicant's former employers and educational institutions. NACO also administers a seven-level rating system to help match an applicant's level of skill against job requirements. Testing is required for the upper levels. NACO also publishes a newsletter, maintains a bulletin board, and tracks the CAD/CAM job market.

Dues are US $50 per year and testing costs $45 to $145, depending on certification level. *Contact: National Association of CAD/CAM Operators, 10801 Hammerly, Suite 220, Houston, Texas 77043; or* **circle 104.**

COMPUTERS

Neural network in hardware

If you thought that neural networks were strictly a software function, think again. Putting all the needed intelligence, artificial or otherwise, on a board with a dedicated processor produces a unit that can learn and respond faster than a neural net program running on a more traditional computer. Shenandoah Systems Co. has accordingly configured the cerebellar model arithmetic computer (CMAC) in hardware for the PC-AT bus.

The CMAC type of neural network is quick to learn and suited to many applications that require an adaptive response in real time. It is basically a table look-up technique for representing complex multiple-input, multiple-output nonlinear functions over particular regions of the function state space. It is taught the appropriate table values by being given a series of inputs and told what the correct answers are. The processor looks at the data and assigns a weight to each input. If it is then given similar inputs it will use the weights to calculate a similar, and one may hope correct, response. If the responses are not correct, the network must be given a new set of input and output vectors.

CMAC neural networks have been used in robot control, signal processing, and pattern recognition applications. They can work on "inverse" problems, determining the input if the output is known. They contain a few features useful for real-time applications such as input/output buffers and support for interrupt-driven software.

The CMAC-AT is designed for use in an IBM PC AT or compatible. It comes with a software driver and demo disk for US $7950. *Contact: Carl-Henry Piel, Shenandoah Systems Co., 1A Newington Park, West Park Drive, Newington, N.H. 03801; 603-433-4787; or* **circle 105.**

HARDWARE

Power in hand

Workstations on a network, computers on a factory floor, and medical instruments are prone to power-related problems. Although power-monitoring products are available to help diagnose what ails them, most cost a lot and their users require experience to interpret the results. Less skill and fewer dollars are needed for the 100G Power Visa, which, plugged into a wall socket, automatically monitors the current's waveform shape, voltage, and frequency. It also detects line-to-neutral and neutral-to-ground impulses and monitors high-frequency noise and ambient temperature. The user can set fault thresholds or rely on the unit's default values and command the unit to print reports either when a fault occurs or every 24 hours.

Perhaps the Power Visa's most valuable feature is its ability to diagnose and isolate the cause of a problem. When a fault is detected, the 100G will compare its waveform to those in a database, determine the probable cause, and suggest solutions. The unit will print, in several languages, advice on solving your power problem and help with using the 100G. It operates at any line voltage from 90 to 290 volts at 50 or 60 hertz.

The CMAC-AT is designed for use in an IBM PC AT or compatible. It comes with a software driver and demo disk for US $7950. *Contact: Carl-Henry Piel, Shenandoah Systems Co., 1A Newington Park, West Park Drive, Newington, N.H. 03801; 603-433-4787; or* **circle 105.**

SOFTWARE

Free scientific software

Scientists and engineers looking for inexpensive software should investigate the Laser and Science Bulletin Board. They will find IBM PC-compatible software in such diverse subjects as astronomy, biology, chemistry, electronics, laser and general physics, and even project management. Some of the programs are in the public domain, the others are either freeware or shareware. Uploads donated by users are always welcome and posted with due credit to the donor.

Use of the bulletin board is free but a password, issued by mail only, is required. *Contact: R. T. Pitlak, 1639 Valecroft Ave., Westlake Village, Calif. 91361; or* **circle 111.**

Coordinator: Dennis DiMaria
Consultant: Paul A.T. Wolfgang, Boeing Helicopters

Forum

(Continued from p. 6)

doesn't bother them.

Some 10 or 20 years ago, the "new math" was all the rage. After raising a generation of mathematical illiterates, new math was pretty much discredited. The problem is that those same mathematical illiterates are now teaching, writing textbooks, writing curricula, and teaching other teachers. My son's high school chemistry book from last year is a good example; I found roughly one factual error on every two pages.

These are not isolated instances. I work with two dozen other engineers, and we often compare notes and shudder at the stupidities taught to our children.

This brings up an interesting point—in elementary and high school level math and science, it is relatively easy to tell the difference between right and wrong. If the authors are so incompetent that they cannot keep their facts straight in these subjects, what has been done in history, English, or other fields, where the distinction between truth and falsehood is less obvious?

In many communities, teachers now command salaries as high as $75 000, higher than many of the small businessmen, engineers, and other professionals in the area who work much longer hours, under much greater pressure, and are much more accountable to produce results. These salaries and working conditions, and the prospect of even more income from book royalties, have attracted charlatans and incompetents. Instead of being looked up to, the teaching profession today is the object of derision. See what Nobel Prize-winning physicist Richard Feynman had to say about educators and textbooks in his autobiography, *Surely You're Joking, Mr. Feynman*, as an example.

The title of a recent editorial in our local newspaper summed it up very well: "Teachers can't teach what they don't know." Amen.

Peter A. Stark
Mount Kisco, N.Y.

Correction

On p. 58 of the Feb. issue, the frequency range for 12-gigahertz satellite downlinks in International Telecommunication Union Region 2 (North and South America) should be 11.7–12.2 GHz.

Readers are invited to comment in this department on material previously published in *IEEE Spectrum*; on the policies and operations of the IEEE; and on technical, economic, or social matters of interest to the electrical and electronics engineering profession. Short, concise letters are preferred. The Editor reserves the right to limit debate on controversial issues. Contact Forum, *IEEE Spectrum*, 345 East 47th Street, New York, N.Y. 10017 U.S.A.

READER GUIDE TO PRODUCTS AND SERVICES

HOW TO ORGANIZE FOR GOVERNMENT ACTIVITIES AT THE STATE LEVEL

The IEEE U.S. Activities State Government Activities Committee has developed a publication entitled "How to Organize for Government Activities at the State Level." This brochure is one response to the need to develop an organizational structure at IEEE's Region and Section levels to provide a cohesive mechanism for communicating and working with state and local government agencies. Included are model organizational structure and organizational guidelines for State IEEE Legislative Advisory (SILA) groups as well as a model intersociety structure and model bylaws for SILAs that want to lead area intersociety efforts, or state government affairs organizations.

For a complimentary copy of the brochure, CIRCLE #71 on the Reader Service Card.

INNOVATIVE NEW SERIES

IEEE Educational Activities is publishing two new monograph series for engineers in easy-to-use handbook format.

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First-hand professional experiences of recognized experts offer engineers the opportunity to learn from the mistakes and successes of their colleagues. The first two titles—to be published in Spring 1991—are **Electric Transmission Systems** by John Cassava and **Local Oxidation of Silicon** by Else Kooi.

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• Diffusion of Impurities • Surface Structure and Oxidation • Ion Implantation • InGaAs and InGaAsP: Miscellaneous Properties • Exploitation of InP in Devices.

ISBN 0 85296 491 9, Casebound, 1991
425 pages, 280 by 210 mm, $250.00

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PRE-EMPLOYMENT PATENT AGREEMENTS

Employed Engineers: Who Owns Their Inventions? was published by IEEE United States Activities as a guide for leaders of professional activities groups. This booklet explains a number of pre-employment patent agreements and what they mean to the employed inventor. Detailed guidance on the assignment of rights, forms of reward, confidentiality of employer information, disclosure of prior inventions, and a sample agreement are included.

Copies are on sale to members through the IEEE Service Center, Box 1331, 445 Hoes Lane, Piscataway, N.J. 08855-1331; 201-981-1393 or 800-678-IEEE. Ask for Catalog No. UH0147-9. Price is US $5.00 for members and US $6.50 for nonmembers.

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IEEE-USA's Pensions Committee has assembled an informative chartbook, *Understanding Pensions*, as an educational service to IEEE's U.S. members.

Understanding Pensions is not just for those soon to retire. The chartbook is for everyone who wants to begin planning ahead for a more financially secure retirement. And since the accumulation of retirement income takes a considerable period of time, it's very important that today's increasingly mobile workers learn as much as they can, as soon as they can, about how pensions work.

The chartbook was designed for use by engineers, scientists, and other professionals who want to learn more about pensions and how the nation's voluntary private pension system operates. *Understanding Pensions* provides 58 visuals, each accompanied by text containing basic factual information, informed opinion, and practical advice.

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IEEE-USA has revised and updated a career guidance brochure, *Your Career in the Electric, Electronics, and Computer Engineering Fields*. The brochure is distributed to high school and college students who are interested in exploring careers in electrical, electronics, or computer engineering. Copies are also sent to high school counselors, libraries, career counseling centers, and other interested institutions and individuals.

IEEE members may obtain up to 25 copies free of charge for distribution at local student events by contacting the IEEE-USA Office in Washington, D.C. If more than 25 copies are required for a single event, the balance must be purchased at $0.75 each. Individual copies are available free.

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The following listings of interest to IEEE members have been placed by educational, government, and industrial organizations as well as by individuals seeking positions. To respond, apply in writing to the address given or to the box number listed in care of *Spectrum* Magazine, Classified Employment Opportunities Department, 345 E. 47th St., New York, N.Y. 10017.

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Academic
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Academic Position Open. College of Computer, King Saud University invites applications for open positions at the rank of lecturers, assistant professors, associate professors and professors in the Computer Engineering, Computer Science and Information Systems Departments for the academic year starting Sept., 1991. A strong commitment to teaching on the graduate and undergraduate level and the development of research program in the above areas is required. Rank and Salary are highly competitive and based upon experience and qualification. Send complete resume to Dean, College of Computer, King Saud University, PO Box 51178, Riyadh 11543, Saudi Arabia.

Texas **A&M University.** The Electrical Engineering Department has several openings for tenure track faculty at all ranks. Applicants must have a Ph.D. degree. For senior positions, the individuals should have a proven record of scholarly contributions, and for junior positions, demonstrated potential for quality research and teaching is necessary. The salary is competitive and commensurate with qualifications and experience. The Department has 1300 undergraduate students, 350 graduate students and a faculty of 56. Currently the active areas of graduate programs include digital and analog microelectornics , electronic and magnetic materials and devices, electromagnetics, micorowave engineering, computer engineering, electrooptics, telecommunications, controls, signal processing, electric power systems, and power electronics. Qualified individuals having expertise in any of these research areas are urged to apply. The Department has a particular interest in hiring outstanding faculty in the areas of computer engineering, microelectronics, electronic materials, electromagnetics, microwave engineering, power systems automation, solid state electronics and signal processing. Applicants should send a complete resume, including names and addresses of three references to Dr. J.W. Howze, Department Head, Electrical Engineering Department, Texas A&M University, College Station, TX 77843. Texas A&M University is an equal opportunity/ affirmative action employer, and actively seeks the candidacy of women and minorities.

Wright State University, Department of Computer Science and Engineering invites applicants for tenure-track and visiting faculty positions at all ranks. The successful candidate must have a Ph.D. in computer science, computer engineering, or equivalent background and have demonstrated forward looking and creative research. Further desired attributes include: capability to direct Ph.D. candidates in computer science or computer engineering and the ability to acquire funds and/or direct research projects. Preferred technical areas are distributed systems, networking, and database, but other areas will be considered. Rank and competitive salaries are determined by qualifications and experience. The University is located in a high technology environment among industrial/military research and development facilities, including Wright Patterson Air Force Base and NCR. Department strengths include a fully networked Unix environment of Sun & DEC workstations; Cray access; graduate laboratories in AI, optical computing, neural networks, and robotics; established research programs; industrial/military support; degree programs in both computer science and computer engineering; and a large graduate student population. Please submit a detailed resume including names of three references to: CSNET address—amcaulay@cs.wright.edu or Alastair D. McAulay, NCR Distinguished Professor and Chair, Department of Computer Science and Engineering, Wright State University, Dayton, Ohio 45435. Pending availability of funding, reviewing for positions will begin February 15, 1991 and continue monthly until positions are filled or until September 1, 1991. An Equal Opportunity/Affirmative Action Employer.

Stocker Visiting Chair in Electrical and Computer Engineering at Ohio University. Applications and nominations are being accepted for the position of Stocker Visiting Professor in Electrical and Computer Engineering (ECE). The ECE Department at Ohio University has twenty full-time and four part-time faculty, 450 undergraduate students and 80 graduate students. External research support in ECE exceeds $2.3M per year, a large portion of which comes via the Avionics Engineering Center, a unit of ECE. The ECE Department is housed in the $15M Stocker Engineering Center. The Stocker Chair position is supported through the Stocker Endowment, presently worth more than $13M. Qualifications for consideration for the Stocker Chair position include noteworthy achievements in research and teaching or industry/government. The individual selected for this position is expected to teach, participate in Departmental research, and be available to present and conduct invited seminars/lectures at various universities, including O.U. The maximum term of appointment for this position is three years; a lesser term can be negotiated. Stocker Professors are provided part-time secretarial support, a travel allowance, special office accommodations, and equipment/supplies support, if needed. In addition, modest furnished living quarters, specifically designated as Stocker Chair Apartments, are available for Stocker Professors and their spouses. Salary for the positions is negotiable. The ECE Stocker Chair position is ideal for a person who wishes to take leave from his/her present employer. Applications and nominations will be accepted until the positions is filled. Please send a resume with at least three references or your nomination to Dr. Jerrel R. Mitchell, Stocker Center, Ohio University, Athens, OH 45701-2979. Preference will be given to U.S. citizens and permanent residents. Ohio University is an equal opportunity and affirmative action employer.

Faculty Position. Cooper Industries Professor of Electrical Engineering: The Electrical and Computer Engineering Department at Ohio University is continuing its search for a senior tenure-track faculty member. The Cooper Industries Professor of Electrical Engineering will be expected to teach and develop a sponsored research program in power electronics and.or industrial controls. A demonstrated ability to interact with industrial sponsors is essential. The successful candidate is expected to take a leading role in developing a multi-disciplinary program in computer-integrated manufacturing. Candidates must have an earned Ph.D. in engineering, a demonstrated record of teaching (undergraduate and graduate) and significant experience in promoting and conducting sponsored research. Interviews will continue until the position is filled. Send resume and a list of four references to H.W. Hill, Jr., ECE Department, Ohio University, Athens, OH 45701-2979. Ohio University is an equal opportunity, affirmative action employer.

Princeton University: The Department of Electrical Engineering invites applications for a full time, tenure-track faculty position. The disciplines of particular interest are: Computer Engineering, with a specialization in computer architecture; and Digital Signal Processing, with a specialization in video and image processing. Please send a complete resume, a description of research and teaching interests and names of three references to Professor Stuart Schwartz, Chairman, Dept. of EE, Princeton University, Princeton, NJ 08544. Princeton University is an equal opportunity/affirmative action employer.

Worcester Polytechnic Institute—The EE Department invites applications for tenure track faculty positions at the Assistant or Associate Professor level in the following areas: Computer Engineering, Data Communications, Ultrasonics, and Microwave devices. Candidates must possess an earned doctorate, and will be expected to have a strong commitment to high quality undergraduate and graduate engineering education, as well as to development of a research program. Applications from women and underrepresented groups are especially invited. Worcester Polytechnic Institute is a technical university offering project-oriented programs in Engineering, Science and Management, WPI is located in the high-tech region of central Massachusetts, with an enrollment of 2,500 undergraduate and 400 full-time graduate students. The EE department has 24 full-time tenure-track faculty, and strong undergraduate, graduate and research programs. Please send a statement of your research and teaching interests, a resume, and a list of three references with addresses and telephone numbers to: Dr. John A. Orr, Head, Department of Electrical Engineering, Worcester Polytechnic Institute, Worcester, MA 01609. WPI is an equal opportunity affirmative action employer.

The University of Texas at Austin, Department of Electrical and Computer Engineering, is accepting applications for a tenured faculty position with the rank of professor in electromechanics/electromagnetics. Duties will include leadership of an internationally competitive research program, program development in classical electromagnetics, and the teaching of undergraduate and graduate level courses. Interested applicants are invited to send resumes which detail their past professional accomplishments, and which include the names and addresses of at least three references, to Dr. Mario J. Gonzalez, Chairman, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, TX 78712-1084. The University of Texas at Austin is an Equal Opportunity/Affirmative Action Employer.

Indiana University—Purdue University at Indianapolis (IUPUI) invites applications and nominations for the position of Dean of the Purdue School of Engineering and Technology. The successful candidate will have an earned doctorate in engineering or related fields, have an estab-

lished record of research and teaching sufficient to merit the rank of professor in the School, have proven administrative experience, and demonstrate an understanding of the relationship between engineering and technology programs. The School has 70 full-time faculty in eight departments offering coursework leading to Purdue University degrees in technology and engineering, including masters degrees in electrical and mechanical engineering. Two new facilities are under construction and should be completed in 1993. Review will begin in March 1991 and continue until the position is filled, preferably by June 1991. Send nominations or applications to: Professor Thomas Lanz, BS 3024C, IUPUI, 801 West Michigan Street, Indianapolis, Indiana 46202-5151.

Iowa State University. The Department of Electrical Engineering and Computer Engineering invites applications for anticipated tenure-track faculty positions at all ranks beginning Fall 1991 semester. The primary need is for specialization in the areas of communications/signal processing, computer networking/data communications, control, microelectronics, and power. Responsibilities include teaching, research and outreach. Salary and rank are commensurate with qualifications and experience. Applicants must possess a doctorate degree with a demonstrated potential for research. Applications should include a resume with a statement of teaching, research, and outreach interests, as well as a list of at least three (3) references. Applications should be sent to: Dr. John Wm. Lamont, Chairman of Faculty Search Committee, Department of Electrical Engineering and Computer Engineering, Iowa State University, Ames, Iowa 50011. Iowa State University is an Equal Opportunity/Affirmative Action Employer.

The University of Toledo. The Electrical Engineering Department invites applications for a tenure track assistant professor position in Satellite Communications. A Ph.D. in electrical engineering is required. Preference will be given to those candidates who have a demonstrated record and the potential for attracting externally funded research. Responsibilities include undergraduate and graduate teaching and research. State University with 24,000+ students including 2,200 students in B.S., M.S. and Ph.D. engineering programs. Send applications with resumes containing names and addresses of three references by April 30, 1991 to Dr. Kai-Fong Lee, Chairman of Electrical Engineering Department, The University of Toledo, Toledo, Ohio 43606-3390. Non-U.S. citizens must indicate their immigration status. The University of Toledo is an Equal Opportunity/Affirmative Action Employer.

Cooper Union. One tenure track position at the assistant professor level in The Department of Electrical Engineering. Duties include teaching undergraduate courses in electronics, directing undergraduate electronics projects, and supervising master's theses candidates. Research is encouraged through the Cooper Union Research Foundation. Only candidates with a strong interest in laboratory development should apply. Ph.D. required. Candidates within one year of completion of this degree will be considered. Please contact Melvin Sandler, Chairman of Electrical Engineering, Cooper Union, 51 Astor Place, New York, N.Y. 10003. Cooper Union is an equal opportunity/affirmative action employer.

Stanford University Joint Professorship (Research) Geophysics and Electrical Engineering. The departments of Geophysics and Electrical Engineering are jointly searching for a research professor in the area of electromagnetic field measurements, data processing and interpretation. The appointment will be evenly split between the two departments. We are looking for a specialist with expertise in EM measurements in the ULF range (around 1 HZ) with interest in piezoelectricity, magnetostriction and electrical conductivity of the earth's crust in general and specifically their application to earthquake phenomena. Experience should include experimental design, instrument construction and data acquisition. Background in lower ionosphere, electrical currents, and long period geomagnetic variations is also desirable. Because this research faculty position needs to be totally supported by grants and contracts, a demonstrated track record in raising substantial research support is essential. This appointment is for a five-year period and is renewable. If interested, please write to: Professor Amos Nur, Department of Geophysics, Stanford University, Stanford, CA 94305-2215. Stanford University is an equal opportunity employer and encourages the application of qualified women and minority candidates.

Physicist, Assistant Research. Low-temperature processing of silicon and opto-electronic materials, photon assisted deposition and etching processes, chemical vapor deposition of various silicon compounds, thick and thin film micro-circuit engineering, computer aided design and simulation of novel solid state devices and circuits. Req: Ph.D. in Electrical Engineering with at least 1 yr. exp. in above activities. Salary: $41,600-52,900, depending on exp. Job site & interview in La Jolla, California. Send this ad & your resume to Job #NOF 1109. PO Box 9560, Sacramento, CA 95823-0560 no later than April 30, 1991.

California State University, Los Angeles—Full Time Temporary Assistant or Associate Professor. Computer hardware and applications. MS degree in Electrical Engineering or related field required. PhD, related industrial and teaching experience highly desirable. Application Deadline—March 25, 1991 for first consideration. Send application to Dr. Martin S. Roden, Chair, Electrical and Computer Engineering, California State University, Los Angeles, CA 90032. Finalists will be asked to solicit letters of reference. For further information, call (213) 343-4470. AA/EEO Employer. Minorities and women strongly encouraged to apply.

Assistant or Associate Professor of Electrical Engineering, Tenure Track. The University of Southern Maine invites applications for a tenure track position at the assistant or associate professor level from persons with a strong commitment to undergraduate teaching and scholarly work in a small but rapidly growing department. A Ph.D. in electrical engineering or a related discipline is required. Primary interest is in electrical power and related areas, but all areas of specialization will be considered. The location is Gorham, a lovely suburb of Portland which is Maine's cultural and industrial center. The department maintains close ties to industrial firms in the area. Screening of applicants will begin immediately and continue until position is filled. Starting date is September 1, 1991. Send curriculum vitae with three references to: James W. Smith, Chair Department of Engineering RE: 101, University of Southern Maine, 37 College Avenue, Gorham, ME 04038. USM is EEO/AA Employer.

McGill University—The Department of Electrical Engineering of McGill University is seeking candidates to fill a tenure-track faculty opening in electromagnetics. Applications are invited from persons who are dedicated to teaching at both the undergraduate and graduate level, and who have outstanding research potential and demonstrated achievements in the field of numerical electromagnetics. Individuals with expertise in wave propagation in matter are particularly encouraged to apply. The Department has a research group in CAD for Electromagnetics with an international reputation, and the incumbent will be expected to integrate into this group. Candidates must have an earned Ph.D. degree or equivalent experience. Graduation from an accredited engineering school is desirable. Please send a resume and a list of 3 references to Professor Nicholas C. Rumin, Chairman, Department of Electrical Engineering, McGill University, 3480 University St, Montreal, Quebec, Canada, H3A 2A7. In accordance with Canadian Immigration requirements, this advertisement is directed in the first instance to Canadian citizens and permanent residents of Canada. Applications from others are welcomed, however, consideration of such candidates must be deferred until a Canadian search has been completed.

Research Scientist—The position is in the area of III-V semiconductor materials growth by molecular beam epitaxy (MBE) and metalorganic MBE (MOMBE). Responsibilities include system maintenance, modification to improve performance, and supervision/instruction of graduate students in the use of molecular beam epitaxy system and independent original research. A Ph.D. in electrical engineering, physics or related field required. At least two years of scientific research is required, which may be a combination of academic and work experience but must include crystal growth using a Vacuum Generators MBE system, in-situ and ex-situ characterization techniques for III-V compound semiconductor and heterostructures. Salary $35,000 per year. Qualified applicants send resume or application letter with ad by April 20, 1991 to: AZ DES Job Service Attn: 732A RE: 5277473 P.O. Box 6123, Phoenix, AZ 85005. Job Location Tempe, AZ. Emp. pd. ad. Proof of authorization to work in U.S. required if hired. Affirmative action equal opportunity employer.

The Department of Electrical Engineering, The University of British Columbia, invites applications for at least two tenure-track appointments as Assistant Professor in the general area of electronics or microwave circuits. Areas of interest include III-V semi-conductor devices, analog electronic circuits including analog VLSI or integrated electronic sensors, and microwave or millimeter wave devices and circuits. A Ph.D. is required. Industrial and/or teaching experience would be useful. The successful applicant would be expected to pursue research vigorously, and to teach at the graduate and undergraduate levels. Collaboration with other departments will be facilitated through the new Advanced Materials and Processing Laboratories. Salary is commensurate with qualifications and experience. Start-up funding is available for purchase of equipment and support of graduate student research assistants. The position is available as of July 1, 1991. Priority will be given to applications received before May 31, 1991. To apply, send curriculum vitae, reprints of published papers, names of at least three references, and state eligibility for employment in Canada to: Dr. R.W. Donaldson, Head, Department of Electrical Engineering, The University of British Columbia, 2356 Main Mall, Vancouver, B.C., Canada V6T 1W5. The University of British Columbia encourages qualified women and minority applicants. In accordance with Canadian Immigration requirements, priority will be given to Canadian citizens and permanent residents of Canada.

Oklahoma State University—School of Electrical and Computer Engineering. Tenure track faculty positions are available at all levels in the areas of energy systems, controls, communications, photonics, signal processing and computer systems. A doctorate is required. A dedicated staff is available to assist faculty in the preparation of proposals and in the identification of potential funding sources. Rank and salary will be commensurate with experience and qualifications. Positions will remain open until filled. Send resume, sample publications, a statement of research interests and the names of three references to James Baker, Head, Electrical and Computer Engineering, Oklahoma State University, Stillwater, OK 74078. Phone (405) 744-5151, FAX (405) 744-6187. An EEO/AA employer.

South Dakota State University has two open Assistant Professor positions in Electrical Engineering. PhD in EE or related discipline preferred. Will consider persons with an MS in EE plus 30 additional graduate semester credits and 3 years full time relevant experience. Prefer relevant significant industrial experience, earned BSEE degree from, or evidence of significant teaching in, ABET accredited program. Tenure track contingent upon qualifications. Must have effective English communication skills. Desire demonstrated teaching skills, a record of sponsored research participation, the potential to obtain external research funding and demonstrated expertise in one or more of the following areas: electromagnetics, microelectronics, microprocessor systems, or electronic materials and devices. Other technical specialties will be considered. Proposed appointment date is August 16, 1991; however, review of applications will begin on May 15, 1991 and continue until all positions are filled. Brookings, a city of 16,000 on the eastern edge of the state, is within 4 hours driving time of Minneapolis-St. Paul. The area is known for its outdoor recreational activities. For more information and an application form, write Dr. Virgil G. Ellerbruch, Department Head, Electrical Engineering Department, Box 2220, SDSU, Brookings, SD 57007-0194. SDSU is an Affirmative Ac-

tion/Equal Opportunity Employer. (Male/Female). Women and minorities are encouraged to apply. Proof of eligibility for employment required by the Immigration Reform and Control Act of 1986.

Electrical Engineering Faculty Position. The Department of Electrical Engineering at the University of Alaska Fairbanks invites applications for a faculty position in the area of electric power. A Ph.D. is required. The department provides a high quality program of study at the bachelor's and master's degree levels. An interdisciplinary Ph.D. degree program can be arranged for interested students. Excellence in instruction is recognized and strongly supported as is faculty participation in engineering research. Professional registration or the ability to become registered within three or four years is strongly desirable. Effective English language communication skills are essential. Engineering facilities include a VAX 8800, numerous mini and microcomputers and support facilities for electrical engineering research. Salary and benefits are excellent. Applications should be postmarked by May 30, 1991. Submit applications to: Dr. John Aspnes, Head, Department of Electrical Engineering, School of Engineering, 539 Duckering Building, University of Alaska, Fairbanks, Alaska 99775. Preference will be given to U.S. citizens and permanent residents. Your applications for employment with the University of Alaska may be subject to public disclosure if your selected as a finalist. The University of Alaska is an Equal Opportunity/Affirmative Action Employer and Educational Institution.

The University of Michigan. Research scientist position in submillimeter-wave receivers and systems. Ph.D. in electrical engineering, physics or astronomy, with experience in millimeter/submillimeter-wave instrumentation. Send resume to Dr. F.T. Ulaby, 3228 EECS Bldg., Univ. of Mich., Ann Arbor, MI 48109-2122. A nondiscriminatory/affirmative action employer.

Faculty Position: Electrical Engineer: This position comes under the auspices of the Cooperative Developmental Energy Program (CDEP) and is contingent upon External funding. This position is dedicated to the Fort Valley State College-University of Nevada Las Vegas 3+2 dual degree Program. Qualifications: The successful candidate must have a Ph.D. in Electrical Engineering and two or more years of teaching experience. Preference will be given to those with interest in utilizing new educational approaches. Major Responsibilities: The successful candidate will teach the beginning level electrical engineering courses; set up electrical engineering laboratories and establish a research program that will involve undergraduate students; consult and interact with colleagues at the Howard R. Hughes College of Engineering at the University of Nevada, Las Vegas on course content; and perform other duties assigned by the Director of CDEP. Salary: Negotiable. Effective Date of Appointment: July 1, 1991 or until position is filled. Application Deadline: May 15, 1991. Application: Send letter of application, resume, official transcript(s) and 3 references to: Dr. George Canty, Head, Department of Chemistry, P.O. Box 4196, Fort Valley State College, Fort Valley, GA 31030. An Equal Opportunity/Affirmative Action Employer.

Senior Scientist: Sunnybrook Health Science Centre, University of Toronto, Research Program in Aging. Will perform original research, collaborate with other scientists and supervise graduate students within focus areas of: (1) biomechanical studies of falls; (2) neuroimaging techniques in the diagnosis of mental dysfunction; and (3) assistive technology to promote mobility and independence. Prospective candidates should have a Ph.D. or M.D., proven research experience; publications and established grants. Applicants should forward their curriculum vitae, quoting file #HC-1001 to: Dr. Geoff Fernie, Director, Research Program in Aging, c/o Personnel Department, Sunnybrook Health Science Centre, 2075 Bayview Ave., Toronto, Canada M4N 3M5.

Faculty Positions—The Citadel, the Military College of South Carolina, in Charleston, solicits applications for a faculty position in Electrical Engineering, with initial appointment for up to two years. Conversion to tenure track, subsequent to appointment, may become possible. The position is at the Assistant or Associate Professor level with a competitive salary commensurate with qualifications. The Ph.D. degree is preferred, and the ability and desire to teach in an undergraduate Electrical Engineering program (including evening classes) are essential. U.S. citizenship or permanent resident status is required. Opportunities for locally supported research are limited, but expanding. Specializations preferred are in the areas of power and communications. Deadline: June 20, 1991, or until positions is filled, with ongoing screening of applications. Starting date: August 20, 1991. Send resume and list of three references to Dr. Harold W. Askins, Jr., Professor and Head, Department of Electrical Engineering, The Citadel, Charleston, SC 29409. Telephone: 803-792-5057.

Faculty Position available in Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, Michigan. Applications are solicited for faculty positions at all ranks. Qualifications include an outstanding academic record, significant involvement in research, a doctorate or equivalent in electrical engineering, computer engineering, or computer science, and a strong commitment to teaching and research. Senior software faculty and faculty in optoelectronics are of particular interest. Please send resume and names of five reference to: Professor George I. Haddad, Chair, Department of Electrical Engineering & Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122. An Equal Opportunity/Affirmative Action Employer.

University of Wisconsin-Madison, Philip Dunham Reed Chair in Electrical & Computer Engineering. The University of Wisconsin-Madison is resuming its search for a highly qualified and internationally recognized scientist or engineer to fill the Endowed Philip Dunham Reed Chair in Electrical and Computer Engineering. Applications or nominations should be sent to: Professor Bahaa E.A. Saleh, Chairman, Department of Electrical and Computer Engineering, University of Wisconsin-Madison, 1415 Johnson Drive, Madison, WI 53706-1691. Previous applications and nominations will be automatically reconsidered. The University of Wisconsin-Madison is an equal opportunity/affirmative action employer.

Faculty Positions in Electrical Engineering. The Department of Electrical Engineering and Computer Science at the University of Wisconsin-Milwaukee invites applications for faculty positions at all professorial ranks. Preferred areas of interest include, but are not limited to, electromagnetics, solid state electronics and VLSI. Qualifications include an earned Ph.D., a commitment to research and teaching and the ability to carry out a funded research program. Applicants for senior positions are expected to have a distinguished record of accomplishment. Applicants should send a resume and the names of at least three references to: J.D. McPherson, Chair for Electrical Engineering, Department of Electrical Engineering and Computer Science, University of Wisconsin-Milwaukee, P.O. Box 784, Milwaukee, WI 53201. UWM is an Equal Opportunity (M/F)/Affirmative Action Institution.

Electronics Engineering Technology. Tenure track faculty position starting August 1991 to teach in several of the following areas: circuits, analog electronics, digital electronics, communications, control systems. Masters degree and three years recent and relevant industrial experience required. Teaching experience and a doctorate desirable. Open until filled. Screening will begin May 6, 1991. Send letter of application, resume, unofficial transcripts and the names, titles, addresses, and phone numbers of three reference to: Prof. David Perkins, Chair, Engineering Technology, University of Southern Colorado, Pueblo, CO 81001-4901. USC is an AA/EO Employer.

Division of Science and Technology School of Microelectronic-Engineering Senior Lecturer (Continuing Appointment) Reference No. F1-91. The programmes within the school provide a coordinated coverage of integrated electronics within applications in the area applied to analogue and digital electronics and solid state physics, communications, computing, digital systems and control systems. The University is expanding its activities in microelectronics and related areas and has developed extensive laboratories which include computer aided design, digital systems and software engineering and control systems. A suite of fabrication facilities (housing an ion implanter, pattern generator and other processing equipment), communications equipment (including weather satellite systems, VHF spectrum analyser etc), laser laboratories and access to extensive physical surface analytical facilities. Newer developments include a number of general purpose research and special project laboratories. It is anticipated that the appointee will possess either extensive industrial or teaching experience and a good research record in the areas of digital systems and/or software engineering. Particular teaching areas include digital circuits and systems and/or software engineering. The pursuit of research in microelectronics is a requirement of this position. The appointee will be expected to commence duties as soon as possible. The appointment may be made at the lower part of the Senior Lecturer salary scale of A$43,984-$51,015 per annum. Applications from both women and men are encouraged. Employment benefits include recreation and parental leave and superannuation. Assistance with removal expenses will be met for appointees from outside Brisbane. A range of child care services is available, though waiting lists may apply. Further details are available from Mr. James R. Walden, Divisional Administrator, to whom applications, including curriculum vitae and the names, addresses and facsimile numbers of three referees should be sent by 28 June 1991. Griffith University, Nathan Qld, Australia 4111. An Equal Opportunity Employer.

Government/Industry
Positions Open

Engineer, Sr. Staff of Quality & Reliability. Plan, dev. & direct Total Quality Control (TQC) system for the company; dev. strategy for quality assurance for IC products; dev. & direct measurements & methodology for reliability test & failure analysis; plan & define quality control system for advanced VLSI wafer fab operations in Taiwan; plan & set-up patent committee and document control center. PH.D. in EE + 3 yrs. in job offered or in engineering required. Must have experience in wafer fab manufacturing, documentation & quality control, BiCMOS, 0.8 Micron process, thin film transfer technology. Must also know advanced MOS technology development and TQC. $4800/mo. Job site interview: Sunnyvale, CA. Send ad with resume to: Job #DB 22008, P.O. Box 9560, Sacramento, CA 95823-0560, no later than 5-1-91.

Tech staff/CAD, fab. & testing of high-Tc superconductor (HTS) & HTS/semiconductor circuits for microwave appl., incl. filters, trans. lines, phase shifters, mixers, antennas & related systems. Reqs. PhD/EE; knowledge of electromagnetic & antenna theory, microwave tech & test apparatus, superconductor phenomena & devices, semiconductor devices & circuits, filter theory, signal analysis, microfabrication tech. FT; $5,000/mo. Job site & interview: Sunnyvale, CA. Send ad & resume application to Job No. SK 2085, P.O. Box 9560, Sacramento, CA 95823-0560 by 4/30/91.

Engineering Senior CAD Engineer Develop & characterize advanced computer models for VLSI and ULSI semiconductor manufacturing process/equipment design, incl. top-down process design, integration, control and diagnosis. Ph.D.'s in either Electronics or Electrical Engr'g. or Electronics Engr'g. & C.S. opr Electrical Engr'g. & C.S. Academic project/research background in statistical/physical modelling and characterization of CVD process/equipment for CAD, integration, control and diagnosis of semiconductor manufacturing, incl. LPCVD thin-film deposition and clean room operations; also C, FORTRAN, UNIX, TCAD simulators, incl. SAMPLE, SUPREM & SPICE and statistical analysis software, icls. RS/1; academic coursework in IC Digital and Analog Design, IC Device and Processing, Probability & Statistics, AI and Expert Systems. $4,700/mo.; 40 hrs./wk. Place of employment and interview: Santa Clara, CA. If offered employment, must show legal right to work. Clip ad and send with resume to: Job No. MD 21090, P.O. Box 9560, Sacramento, CA 95823-0560 not later than May 1, 1991. The company is an equal opportunity employer and fully supports affirmative action practices.

Help Wanted: Senior System Software Engineer. By 5/1/91 Please send resume to: Employment Security Department, ES Division, Att: Job #

CLASSIFIED EMPLOYMENT OPPORTUNITIES

246223, Olympia, Washington 98504. Job Description: Designs, implements and tests complex and high level systems and software for micro computers. Assumes senior responsibility to design the graphics engine for Presentation Manager utilizing MS-DOS, Windows and OS/2 operation systems, "C" and 86 Assembler Series family of languages. Develops and implements font driver to achieve "what you see is what you get" (WYSIWYG) displays for OS/2. Assumes major project responsibility including: 1) requirements and analysis of project specifications; 2) product design; and 3) implementation schedules. Requirements: M.A. or M.S. in electrical engineering, computer science, mathematics or physics. Six months of work experience developing and implementing font technology to achieve WYSIWYG display including design and development of font driver or advanced printer drivers (imaging model). This must include six months of work experience utilizing MS-DOS, Windows and multitasking operating systems, and "C" and 86 assembler series family of languages. Must have legal authority to work in the United States. Job locations: Redmond, Washington, Salary: $37,500-$50,000 per annum, depending on experience, 40 hours per week, flex time. EOE.

Help Wanted: Senior Systems Software Engineer, International Product Group. By 5/1/91 please send resume to: Employment Security Department, ES Division, Att: Job # 245651, Olympia, Washington 98504. Job Description: Designs, implements and tests complex and high level systems and software for micro computers. Assumes senior responsibility to design and adapt graphics business applications software for sale in foreign markets. Utilizes 86 Assembler Series and "C" languages, MS-DOS operating system and IBM PC computer. Designs and modifies graphical user interface software products for international sale. Implements and maintains international kits and development tools for graphics business applications software using streamline editors and parsing languages. Conducts design and code review for adaptation of software for international sale. Assumes major project responsibility including: 1) requirements and analysis of project specifications; 2) product design; and 3) implementation schedules. Requirements: Masters in electrical engineering, computer science, mathematics for physics. Six months work experience in programming or computer software design utilizing MS-DOS operating systems 86 Assembler series and "C" languages, and streamline editors and parsing languages and designing development tools and design, modification of graphical user interface and design and code review. Must have legal authority to work in the United States. Job Location: Redmond, Washington. Salary: $37,500-39,000 per annum, depending on experience, 40 hours per week, flex time, EOE.

Design Engineer—Hard Disk Drives, 40 hrs./wk. 9:00 am -5:00pm, $38,000/yr. Design/modifications of circuits for computer components such as hard disk drives. Establish test parameters for printed circuit boards. Develop custom testing equipment. Train technicians in disk drive repair. MS in Electrical Engineering and Computer Science as well as 3 years experience as a Design Engineer—Hard Disk Drives or as a Design Engineer required. Previous experience must include microprocessor system design, motion and linear control, phase lock loop design, filter design, Graduate coursework must include: Advanced Control Theory; Concurrent Computer Systems; VLSI Design. Must have proof of permanent legal authority to work in the U.S. Send resume to: Illinois Department of Employment Security, 401 South State Street—3 South, Chicago, Illinois 60605, Attention: Len Boksa, Reference #V-IL-2143-B, No Calls, an employer paid ad.

Marmara Research Centre of the Turkish Scientific and Technical Research Council invites applications from scientists and engineers interested in working the lively environment of the best and largest R&D laboratories of Turkey on in-house and contract research projects in the fields of: Basic sciences; Electronics and Communications; VLSI Design; Optoelectronics; Speech Processing; Radio Astronomy; Remotes Sensing; Artificial Intelligence; Computer Engineering; Robotics; Control Systems; Materials; Chemical Engineering; Biotechnology; Environmental Engineering; Energy. The Centre, situated near the exciting and ancient city of Istanbul on the beautiful shores of the Sea of Marmara, is closely associated with academic and industrial establishments in the area. Pleas send your application together with CV and expected salary to: Prof. Nejat Ince, Tubitak Marmara Research Centre, P.K.21, 41470 Gebze-Kocaeli, Turkey. For more information call: (90)199-11678.

Scientific Programmer—Position available to research and design mathematical algorithms that perform steady state electric utility network dispatcher, optimal power flow & voltage scheduler functions on real-time energy management computer systems. Will utilize FORTRAN & "C" to code algorithms & integrate into large, multi-main frame computer system. Must have MS in electrical engineering, with research in real-time steady state operation of large-scale power systems, utilizing linear mathematical techniques to solve dispatcher & optimal power flows. Must have used FORTRAN & "C" programming language for MS level courses & thesis work. Must be a U.S. citizen or permanent resident. Salary $3200/month. Send resume to: Sara Springmeyer, #0-213, Minnesota Department of Jobs & Training, 390 No. Robert St., Room 124, St. Paul, MN 55101. an Affirmative Action Employer.

Senior Research Engineer Conduct R&D in: Glass batch house control system design; glass thickness measurement computer systems; glass tank, bath, and lehr computer data collection systems; process measurement and control systems; tank and bath expert systems. Ph.D. required in Electrical Engineering or Computer Science. Must know C, FORTRAN, Assembler, WDPF languages; VAX, IBM and Apple hardware; Artificial Intelligence expert system design and implementation; and digital, optimum and sensor-based control systems. $44,700/yr. Send resume to New Kensington Job Service, 3 Kensington Square, New Kesnington, PA 15068. Refer to Job Order No. 4143940.

Design Engineer needed to develop and implement series of high voltage and high power density dc-dc converters using hybrid technology to meet military standards and environmental tests. Design high voltage dc-dc converter, transformer, inductor and electromagnetic interference filter. Apply proportional integral control, linear optimal control and adaptive control techniques for dc-dc converter. Develop C language-based software programs utilizing state equation, optimization theory, finite element analysis and numerical solutions to support converter and magnetic designs, to analyze thermal distribution, electrical and mechanical stress and to predict converter steady-state and dynamic responses. Requires a MS degree in Electrical Engineering and 2 years exp. in design high voltage dc-dc converter and electromagnetic interference filter, apply linear optimal and adaptive control techniques, finite element analysis and C language to support converter design. 40 hours work week. $40,200 per year. Position permanently in the U.S. Send resumes by May 1, 1991 to Employment Security Department, E.S. Div., Job No. 248646-C, Olympia, WA 98504. Ad paid by equal employment opportunity employer.

Electrical Engineer, Member of Technical Staff, Resp. for architecture, design, implementation, and debug of digital signal processing software for high-speed PSTN modems; duties incl. analysis and eval. of single and multi-carrier modulation and demodulation schemes and effects of channel impairment; method and algorithm design to implement architecture; design and writing of code on high level languages and assembly, simulation, debug documentation. Reqs. PhD. in E.E. Also reqs. doctoral research conc. and track record of contribution/innovations in audio frequency digital signal processing; also reqs. backgr. in development of complex software using high-level languages and involving at least 10,000 lines of code; knowl. of assembly language programming; info. coding theory; control systems; adaptive systems; design and implementation of computer simulations; communications theory, modulation and demodulation. Salary $55,008/year. Job & interview site: Sunnyvale, CA. Send this ad & a resume to Job #BA26025, P.O. Box 9560, Sacramento, CA 95823-0560 not later than April 30, 1991. Must have legal right to work.

Research Engineer. Resp. for development and fabrication protocols for the "PRONG" microelectrode system and peripheral recording and discrimination system for neural signal processing. Duties incl. design & development of efficient algorithms, software, and hardware to store, process and analyze neural signals, as well as technical documentation. Reqs. a Ph.D. in EE and 1 yr. exp. in biomedical data analysis. knowledge of neural recording & discrimination. IBM PC assembly, "C", and window programming. Education must incl. digital signal processing, detection & estimation theory, stochastic point processes, information theory, and error-correct coding. 40 hours per week at $30,200/yr. Must have legal authority to work in the US. Permanent residents & US citizens only need to apply. Job & interview location—Clarksburg, MD. Mail resume & a copy of this ad to: Maryland Department of Economic and Employment Development, 1100 North Eutaw Street, Room 212, Baltimore, MD 21201. Refer to Job order # 9047347. Ad paid by an Equal Employment Opportunity Employer.

Design Engineer for Central Wisconsin biomedical software & equipment firm to design, develop, improve & maintain software for computer controlled sequence scanner for DNA sequencing and analysis using medical terminology; design algorithms for obtaining discrete data by using a photo-detector and an A/D converter, tracking curved lanes and scanning one laneset after another; processing the data to get the finale sequence, including filtering noises, calling bases, deleting extra bases, filing gaps, shifting data, & checking final sequences. 6 mos. exp. req. in above job duties, along with an M.S. degree in electrical engineering (must have one course each in advanced calculus, numerical analysis, & applied linear algebra). M-F 8AM-5:30PM. $28,000/yr. Must have proof of legal authority to work permanently in U.S. Send resume in duplicate (No Calls) to Alexis Taylor, JO#0389669, Wisconsin Job Service, 206 N. Broom Street, PO Box 7943, Madison, WI 53703-7903.

CAE Software R&D Engineers—Magnetics: Ansoft Corporation is a CAE software leader in the electromagnetics and electronics industries. Ansoft's line of software products—MAXWELL® Software—is marketed worldwide. Ph.D. positions require a Ph.D. in EE with 3+ years experience in FEA and emphasis on magnetics; experience with C++ or C, Unix and X-Windows preferred. MSEE/BSEE positions require 2+ years programming experience, proficiency in C++ (or C), with Unix and X-Windows background; experience with PC and Macintosh and knowledge of FEA desirable. Successful candidates will work in a team environment to carry out projects from conception, design, and implementation to finished product. Send resume to Ansoft Corporation, Engineering Recruiting, Four Station Square, Suite 660, Pittsburgh, PA 15219.

Electronic Engineer—A leading offshore navigation company located in Houston, Texas, has an immediate opening for an electronic engineer with strong R.F./Digital capability. Positions involves supervising technicians and R&D projects used in the radio navigation and GPS satellite industry. Interested applicants should forward their resume to Operations Manager, NCS International Inc., P.O. Box 891266, Houston, TX 77289-1266.

Microwave Engineer/Semiconductor Physisist—The applicant should have a PhD Degree in Electrical Engineering or Semiconductor Physics. He/she should have experience in the area of semiconductor physics with applications to non-linear semiconductor microwave devices. General knowledge in the field of microwave circuit design and in particular the design of low noise and high power microwave transistors will be his/her major responsibility. Our software oriented environment requires the knowledge of a programming language such as C or FORTRAN. Applicants who are willing to work with a motivated research team are encouraged to mail a resume to: Compact Software, Inc., 483 McLean Blvd. & 18th Avenue, Paterson, New Jersey 07504, Attn: Dr. A. Hill.

Staff Engineer: Req. Ph.D. in Computer Science and 3 yrs. exp. design and development of dis-

distributed operating systems, including implementation of distributed file systems, interprocess communication, and kernels. Also requires research in algorithms and concepts for naming in distributed systems. To design and develop a distributed, concurrent object-oriented operating system. $74,000/yr. Job site/interview: Mountain View, CA. Clip ad and send with resume no later than April 30, 1991 to Dept. RASA, P.O. Box 90295, San Jose, CA 95109-3295. Upon hire must show immediate ability to work in the United States.

Research Position Rehabilitation Engineering & Science. The Palo Alto VA Rehabilitation R&D Center invites applicants holding an advanced degree in engineering or the physical or life sciences, for a research position in musculoskeletal biomechanics, neuromuscular control, and rehabilitation. The candidate is expected to become involved in ongoing, funded projects and to develop new research areas as Principal Investigator. Extensive interaction with students and research and medical colleagues at the VA Medical Center and Stanford University is involved. Targeted start date is approximately October 1, 1991. Please send a resume and names and phone numbers of three references to: Kevin McGill, Ph.D., Rehab R&D Center (153), VA Medical Center, 3801 Miranda Avenue, Palo Alto, CA 94304-1200. Salary depends on qualifications. The VA is an equal opportunity employer.

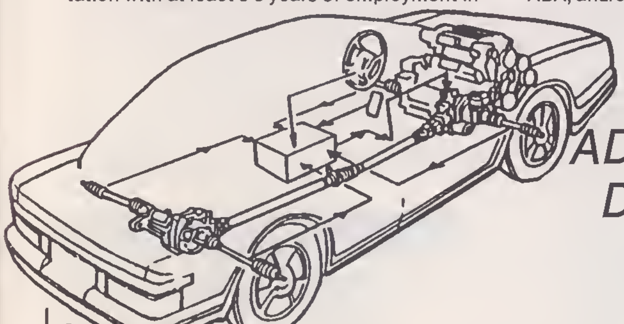
Engineer, Electrical: Control Systems Engineers. Design and detail engineering for DCS (Honeywell) system and PLC system for refinery/chemical installations. Oversee generation of wiring diagrams and design interconnecting cable systems to marshaling panels, local control panels or field devices. Design of analog and digital control signals to Honeywell DCS system, as well as shut down logic signals to PLC system. Generate DCS, PLC system and instrumentation functional and detailed specifications. Utilize DBase III Plus, Lotus, and computer-aided instrument electrical system software to develop an instrument index, data sheets, and loop diagrams. Requires bachelor's degree in electrical engineering or instrumentation with at least 3-5 years of employment in conceptual, basic and detail design engineering for refinery and/or chemical industries. Experience must include estimating, scheduling, engineering, procurement and start-up of DCS (Honeywell) and PLC systems, as well as system configuration, integrated testing, process simulation, and application programming. Experience must also include utilization of Honeywell TDC 3000, including Honeywell interactive graphics generation, database generation for latest Honeywell Controller Process Manager (PM) and Critical Process Controller (CPC). Must be fluent in DBase III Plus, Lotus and an electrical instrumentation software package. Position/interview based out of San Francisco. Position subject to substantial relocation throughout U.S. Present job site, Houston, next sit undetermined. $3,360-4,000/month, DOE. Send copy of this ad with resume to Job number AM 7072, P.O. Box 9560, Sacramento, CA 95823-0560 no later than April 30, 1991. An equal opportunity, affirmative action employer.

Research and development of high-performance, dependable, real-time control computing systems. Responsibilities are to: (1) research, establish, and automate effective algorithms, design methodologies and procedures for scheduling workloads with hard deadlines; and (2) design real-time system level architecture and conduct detailed functional verification and performance analysis. Successful candidate must have a Ph.D. in Computer Science or Computer Engineering, an M.S. or B.S. in Electrical Engineering and at least 4 years related research experience. The candidate must further be able to demonstrate (1) background in fault-tolerant architectures, including STAR, FTMP, SIFT, and FTPP; (2) full understanding of the theories and practices of mathematical programming, scheduling, queueing, and statistical decision-making; (3) at least 3 years hands-on systems in the modeling and analysis of hard real-time experience using GSPN, SAN, CTMC, randomization method and HARP; (4) expertise in modeling, assignment, scheduling and load-sharing of tasks; (5) strong familiarity with VMS or UNIX. Fluent in at least five of these programming languages: Assembly, Fortran, Pascale, C (or C++), Lisp, Prolog, ADA, and/or PL/M; (6) knowledge of data dependency analysis, LAN, control theories, and AI. Proof of legal right to work in U.S. is required. Permanent residents and U.S. citizens only need apply. Work hours are 9:00 am—4:45 pm. Salary range is $46,500 to $55,000. Columbia, MD location. For consideration, send your resume and a copy of this ad to: Maryland Department of Economic and Employment Development, 1100 North Eutaw Street, Room 212, Baltimore, MD 21201. Refer to Job order 9046908. EOE.

Process Engineer: Senior and Intermediate engineers, with a suitable background in either chemistry, electrical engineering, or physics, are sought to develop innovative processing techniques for high power silicon devices. Candidates must have experience in all phases of silicon device processing. The candidate must be motivated and capable of developing innovative, original and efficient designs for solid state systems for use in military and commercial environments. The senior and intermediate engineers will possess an B.S./M.S./Ph.D. along with several year's experience commensurate with the desired position. For confidential consideration, please send your application and resume to Personnnel Department Suite 354 Box 5000 Solana Beach, CA 92075. Candidates must have U.S citizenship.

Detector Technician. The Continuous Electron Beam Accelerator Facility (CEBAF) has an opening for a particle detector/fast electronics technician. Contact Dr. Carlini (804) 249-7123 for information. Applicants should submit a resume specifying position number PR7203 to: Employment Manager, CEBAF, 12000 Jefferson Avenue, Newport News, VA 23606. CEBAF is an Equal Opportunity Employer.

Computer Scientist: Designing and manufacturing automated circuit board inspection systems based on a patented x-ray laminography technology. Requires a computer scientist to create real-time image understanding algorithms. Ph.D. in computer engineering required. One year experience required. Salary of $47k per year plus stock. Job Site/Interview: San Diego, CA. Please send ad and your resume to Job No.: BLW 9086, P.O. Box 9560, Sacramento, CA 95823-0560 no later than May 1, 1991.



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Scanning The Institute

More Federal $$ for R&D?

The Bush administration, despite its agreement with Congress to severely limit spending, has proposed a 13 percent rise in R&D funds to US $75.6 billion. Defense R&D would get the lion's share, with a 14 percent rise to $3 billion within the Pentagon and the Department of Energy. Several initiatives would spur cooperation among Federal agencies in key R&D areas. In particular, the proposed budget allots $638 million, up from $489 million, to the National Science Foundation, the Defense Advanced Research Projects Agency, and six other agencies to work on increasing current computer and communications capability by factors of 1000 and 100, respectively, by the mid-1990s [THE INSTITUTE, April 1991, p. 1].

Self-help for chip industry

A mid-April workshop sponsored by the Government-industry National Advisory Committee on Semiconductors and the White House Office of Science and Technology is to develop a detailed plan for reviving U.S. semiconductor manufacturing. The aim: to boost the industry's worldwide market share. The funding: mostly from industry itself, to the tune of maybe billions of dollars over the next decade. In view: a 1G-bit static RAM and chips for new markets in broadband communications, advanced display system, and intelligent vehicle and highway system [THE INSTITUTE, April, p. 1].

Tradeoffs of global technology

The vanishing technology gap between the United States and other industrialized countries has both beneficial and challenging consequences, according to speakers at the IEEE Power Engineering Society's meeting in February in New York City. Benefits include access to a greater pool of technical talent, greater international technical specialization, and faster spread of superior engineering, managerial, and organizational practices, said Proctor P. Reid, senior program officer at the National Academy of Engineering. Drawbacks include intensified competition between nations and the need in some fields for world-scale markets in order to recoup large investments [THE INSTITUTE, February, p. 6].

A 2.5-Gb/s Olympics first

Warming up for the 1992 summer Olympics in Barcelona, Telefónica de España SA has become the first operator to test a 2.5-gigabit-per-second optical-fiber transmission line system that conforms to the synchronous digital hierarchy (SDH) standard. Already a trial link between Valencia and Cuenca has proved successful. System developer NV Philips of the Netherlands says the standard will make possible a single worldwide transmission system once specific network components become available. SDH innovations include switchable-at-need transmission capacity and the ability to add or drop individual channels. The standard was accepted in 1988 by CCITT [THE INSTITUTE, April, p. 1].

Research grants for IEEE members

The Engineering Foundation in New York City has awarded US $20 000 grants to 10 IEEE members to conduct university research over the 1990-91 school year. Besides funding research, the 76-year-old foundation supports efforts that contribute to public awareness of engineers [THE INSTITUTE, April, p. 6].

Coming in Spectrum

CONSERVING U.S. ENERGY. What role should energy efficiency play in the United States' future? The President's National Energy Strategy disappointed many. Several approaches that have the support of Congress deserve detailed consideration.

SMART CARS ON SMART HIGHWAYS. Intelligent vehicle highway systems are arousing interest around the world because they would reduce travel time, the accident rate, fuel consumption—and pollution. This three-part article describes the goals of such a system, what is in the works in various countries, and what the socioeconomical problems are.

NOTEBOOK COMPUTERS FROM THE INSIDE. Intricate dovetailing of ultraminiature parts fits the new notebook computer—complete with keyboard, video screen, hard drive, and batteries that last for up to three hours—into a 20-by-28-centimeter box weighing less than 3.5 kilograms. Here's how it's done.

BATS, RADAR, AND VLSI. Knowledge of how bats navigate in the dark is pertinent to sonar and radar system design. At Brown University, Providence, R.I., an algorithm based on the tiny mammmals' echo location abilities has been developed and implemented in a very large-scale integrated circuit.

BIRTH OF CMOS. Complementary MOS, today's premier semiconductor memory technology, first went public at the 1968 International Electron Devices Meeting in Washington, D.C. But, as a pioneer from those times recalls, many obstacles had to be overcome before the process could go commercial.

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